LatticeECP/EC Family Data Sheet

LatticeECP/EC Family Data Sheet Introduction

June 2004 **Advance Data Sheet**

Features

- **Extensive Density and Package Options**
  - 1.5K to 41K LUT4s
  - 65 to 576 I/Os
  - Density migration supported
- **sysDSP™ Block (LatticeECP™ Versions)**
  - High performance multiply and accumulate
  - 4 to 10 blocks
    - 4 to 10 36x36 multipliers or
    - 16 to 40 18x18 multipliers or
    - 32 to 80 9x9 multipliers
- **Embedded and Distributed Memory**
  - 18 Kbits to 645 Kbits sysMEM™ Embedded Block RAM (EBR)
  - Up to 163 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 3/2 Class I, II, SSTL18 Class I
    - HSTL 18 Class I, II, III, HSTL15 Class I, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR333 (166MHz)
- **sysCLOCK™ PLLs**
  - Up to 4 analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - SPI boot flash interface
  - 1.2V power supply
- **Low Cost FPGA**
  - Features optimized for mainstream applications
  - Low cost TQFP and PQFP packaging

Table 1-1. LatticeECP/EC Family Selection Guide

Device	LFEC1	LFEC3	LFEC6/ LFECP6	LFEC10/ LFECP10	LFEC15/ LFECP15	LFEC20/ LFECP20	LFEC40/ LFECP40
PFU/PFF Rows	12	16	24	32	40	44	64
PFU/PFF Columns	16	24	32	40	48	56	80
PFUs/PFFs	192	384	768	1280	1920	2464	5120
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	41.0
Distributed RAM (Kbits)	6	12	25	41	61	79	164
EBR SRAM (Kbits)	18	55	92	277	350	424	645
EBR SRAM Blocks	2	6	10	30	38	46	70
sysDSP Blocks[1]	—	—	4	5	6	7	10
18x18 Multipliers[1]	—	—	16	20	24	28	40
V_{CC} Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4
Packages and I/O Combinations:							
100-pin TQFP (14 x 14 mm)	67	67					
144-pin TQFP (20 x 20 mm)	97	97	97				
208-pin PQFP (28 x 28 mm)	112	145	147	147			
256-ball fpBGA (17 x 17 mm)		160	195	195	195		
484-ball fpBGA (23 x 23 mm)			224	288	352	360	
672-ball fpBGA (27 x 27 mm)						400	496
900-ball fpBGA (31 x 31 mm)							576

1. LatticeECP devices only.

Introduction

The LatticeECP/EC family of FPGA devices has been optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP (EConomy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP (EConomy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (EConomy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The Lattice-ECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC family of FPGA devices. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

LatticeECP/EC Family Data Sheet Architecture

June 2004 Advance Data Sheet

Architecture Overview

The LatticeECP™-DSP and LatticeEC™ architectures contain an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR) as shown in Figures 2-1 and 2-2. In addition, LatticeECP-DSP supports an additional row of DSP blocks as shown in Figure 2-2.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional unit without RAM/ROM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM and register functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row. The PFU blocks are used on the outside rows. The rest of the core consists of rows of PFF blocks interspersed with rows of PFU blocks. For every three rows of PFF blocks there is a row of PFU blocks.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM or ROM.

The PFU, PFF, PIC and EBR Blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

At the end of the rows containing the sysMEM Blocks are the sysCLOCK Phase Locked Loop (PLL) Blocks. These PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeECP/EC architecture provides up to four PLLs per device.

Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG™ port which allows for serial or parallel device configuration. The LatticeECP/EC devices use 1.2V as their core voltage.

Figure 2-1. Simplified Block Diagram, LatticeECP/EC Device (Top Level)

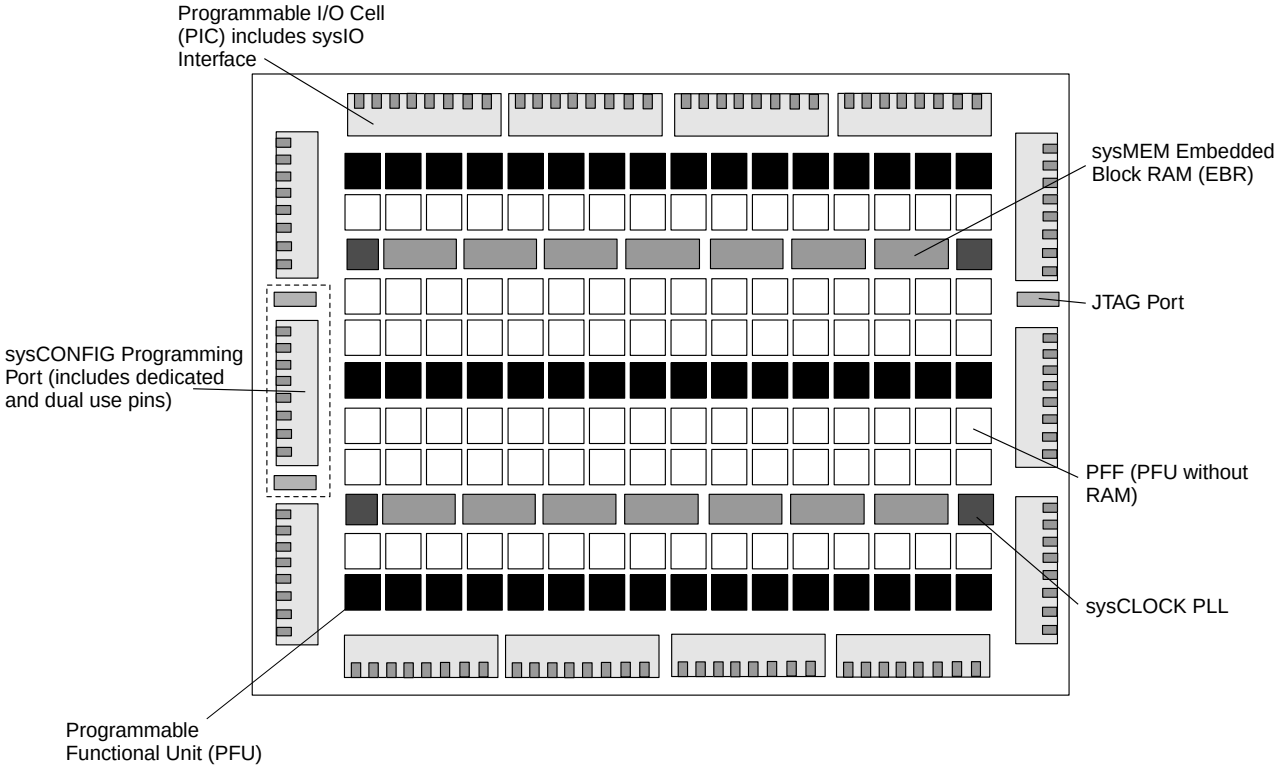
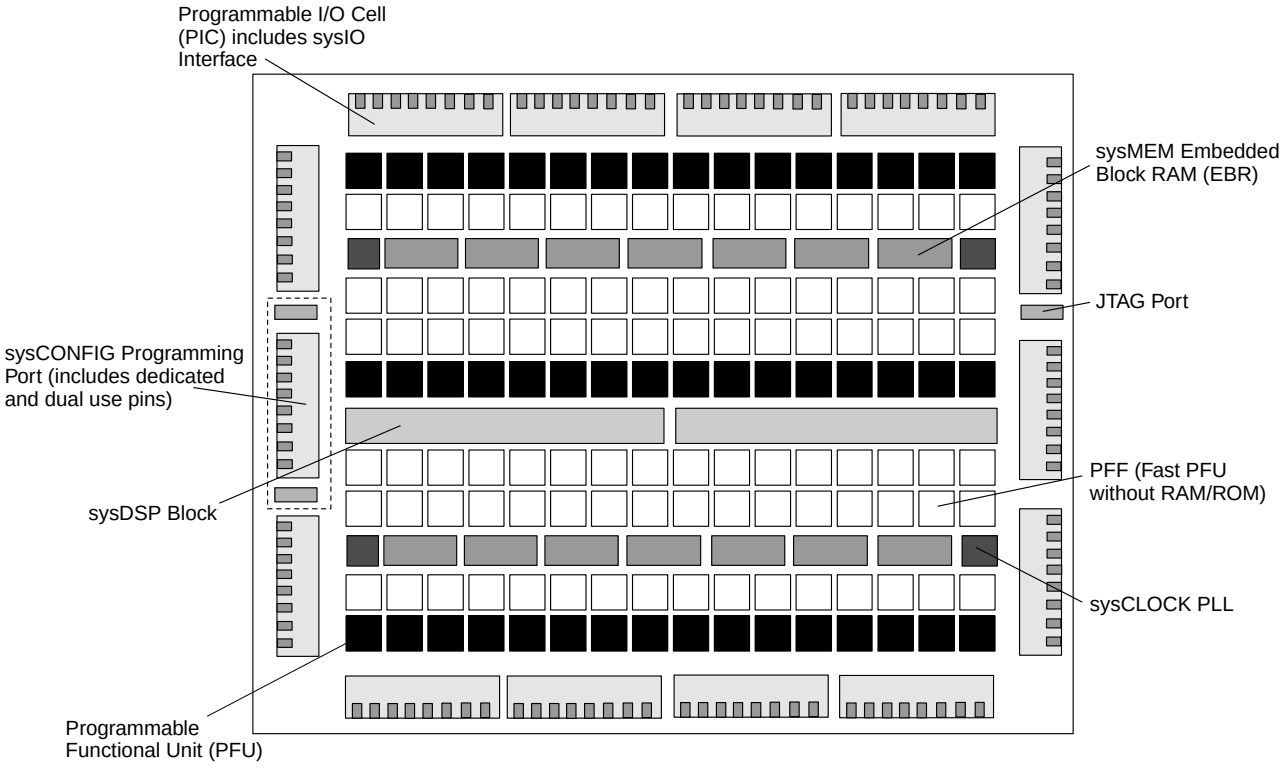


Figure 2-2. Simplified Block Diagram, LatticeECP-DSP Device (Top Level)

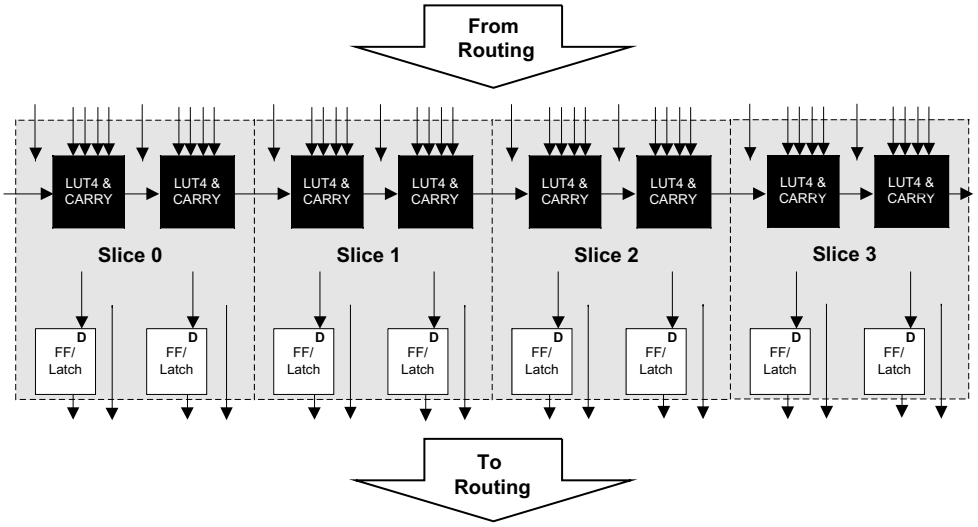


PFU and PFF Blocks

The core of the LatticeECP/EC devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Diagram



Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Figure 2-4. Slice Diagram

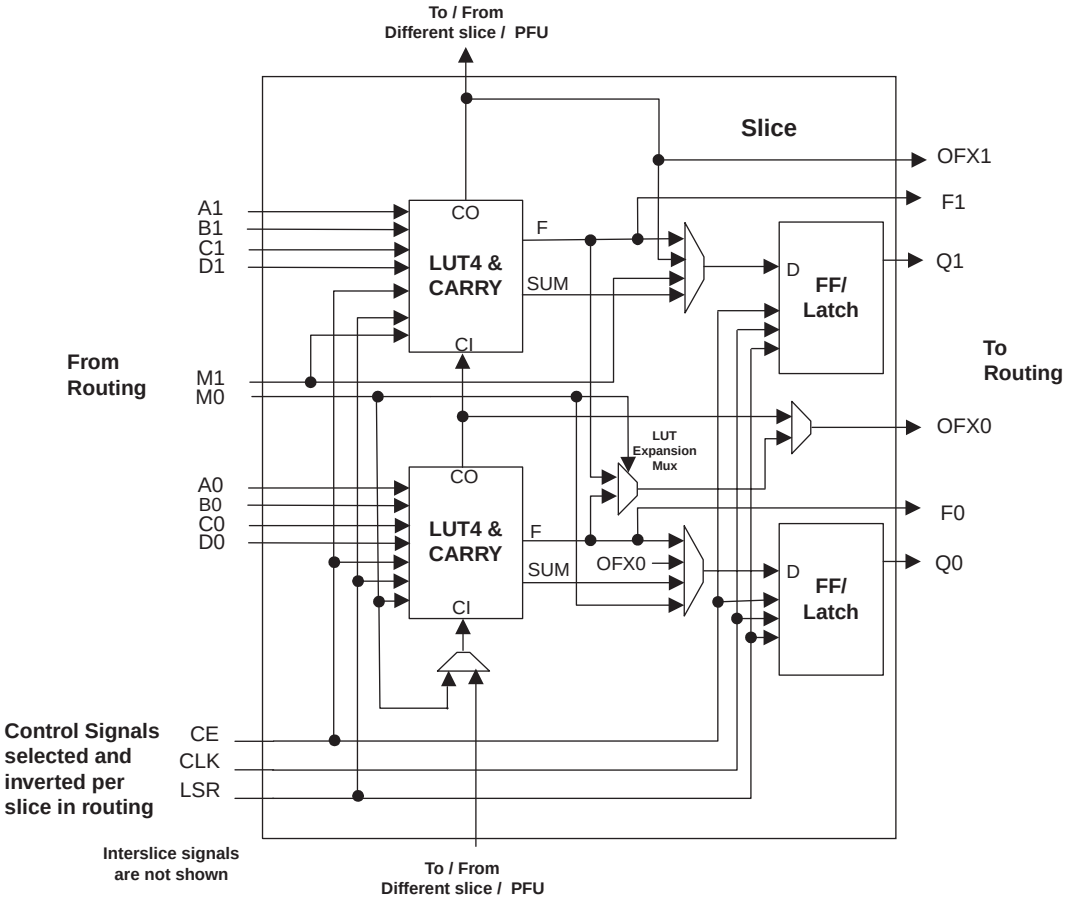


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SPR16x2	ROM16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals: Carry Generate and Carry Propagate are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

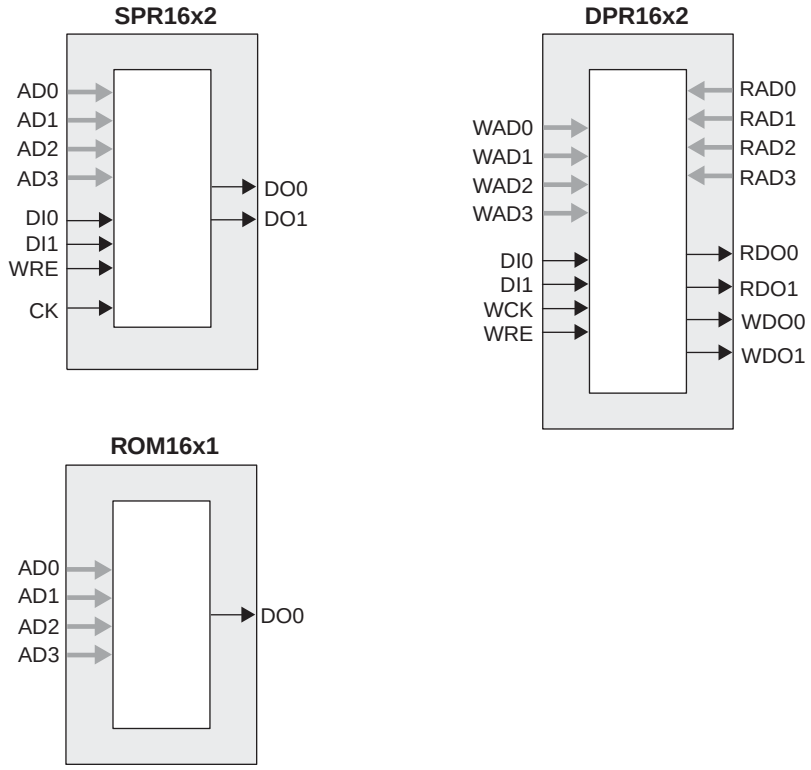
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-5 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on using RAM in LatticeECP/EC devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-5. Distributed Memory Primatives



ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM[1]	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

1. These modes are not available in PFF blocks

Routing

There are many resources provided in the LatticeECP/EC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

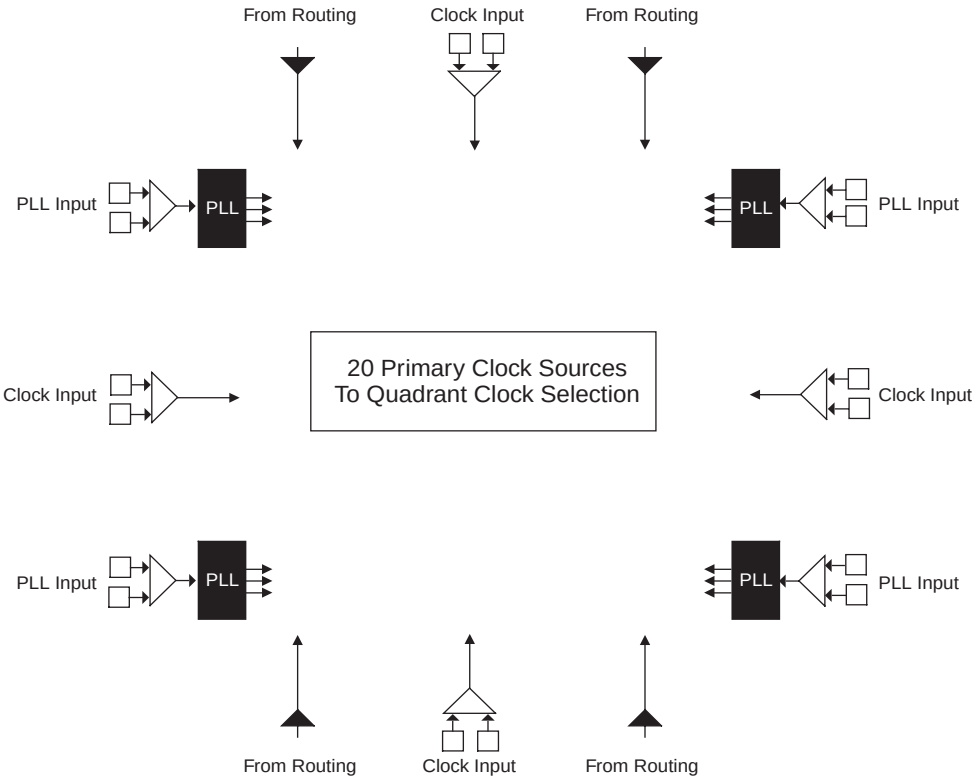
Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeECP/EC devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeECP/EC devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-6 shows the 20 primary clock sources.

Figure 2-6. Clock Sources

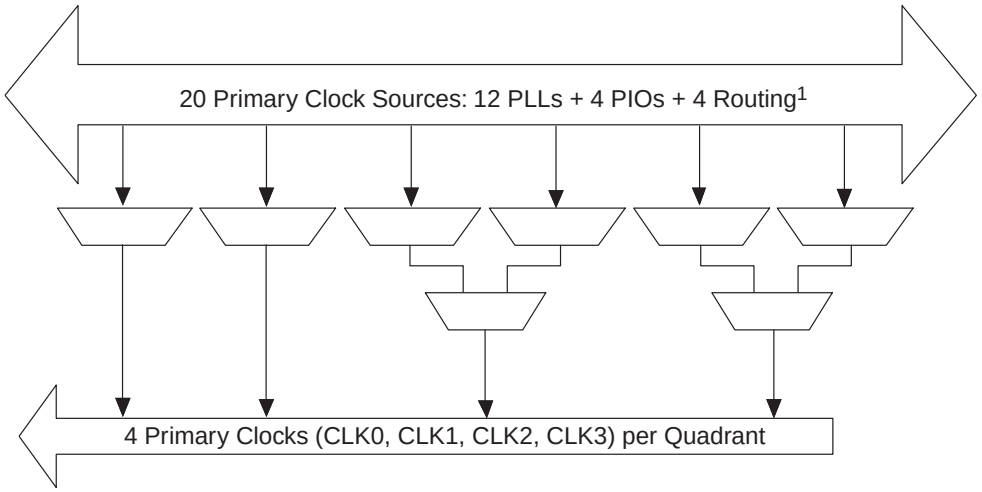


Note: Smaller devices have two PLLs.

Clock Routing

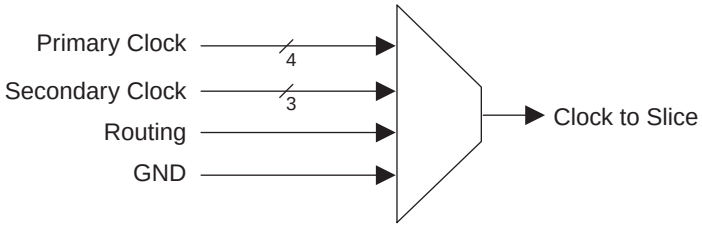
The clock routing structure in LatticeECP/EC devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-7 shows this clock routing. The primary clock lines also feed into a secondary clock network (not shown). The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fan out data. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-8.

Figure 2-7. Per Quadrant Clock Selection



1. Smaller devices have fewer PLL related lines.

Figure 2-8. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are four sources of feedback signal to the feedback divider: from the clock net, from output of the post scalar divider, from the routing or from an external pin. There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-9 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, port scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-9. PLL Diagram

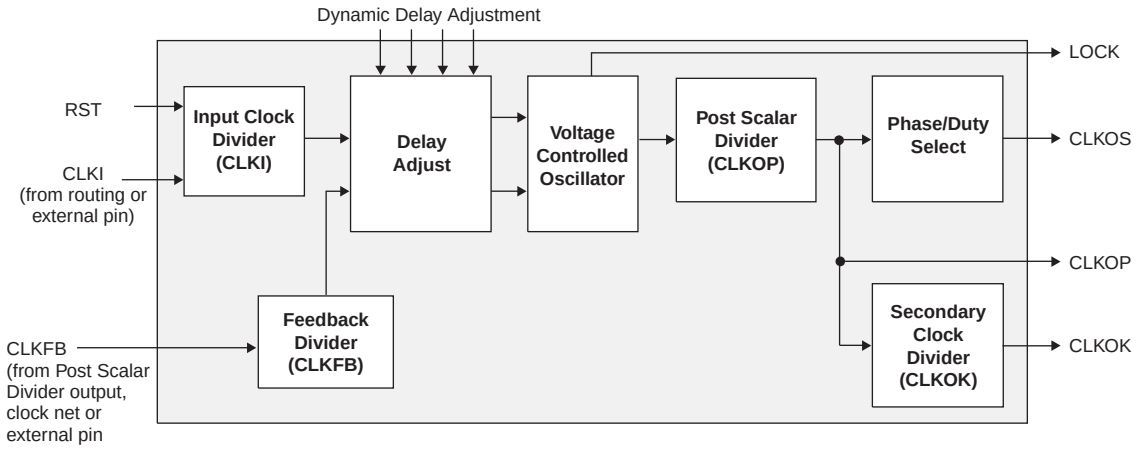


Figure 2-10 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

Figure 2-10. PLL Primitive

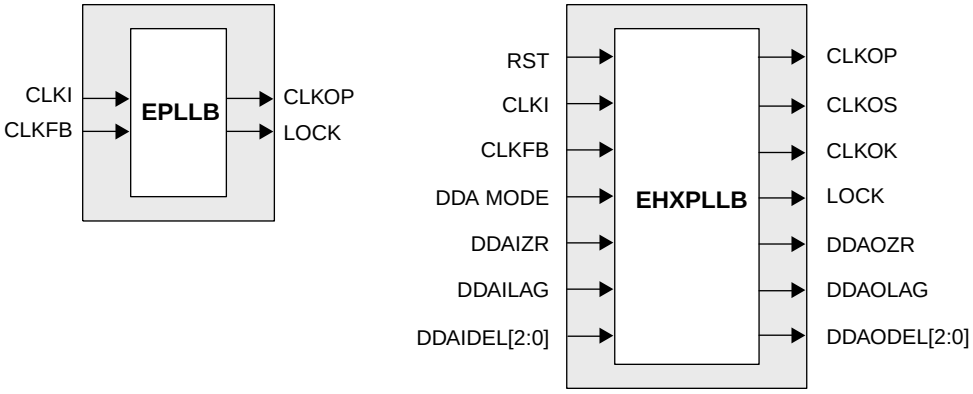


Table 2-5. PLL Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from PLL output, clocknet, routing or external pin
RST	I	“1” to reset input clock divider
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	“1” indicates PLL LOCK to CLKI
DDAMODE	I	Dynamic Delay Enable. “1” Pin control (dynamic), “0”: Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. “1”: delay = 0, “0”: delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. “1”: Lag, “0”: Lead
DDAIDEL[2:0]	I	Dynamic Delay Input
DDAOZR	O	Dynamic Delay Zero Output
DDAOLAG	O	Dynamic Delay Lag/Lead Output
DDAODEL[2:0]	O	Dynamic Delay Output

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

sysMEM Memory

The LatticeECP/EC family of devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

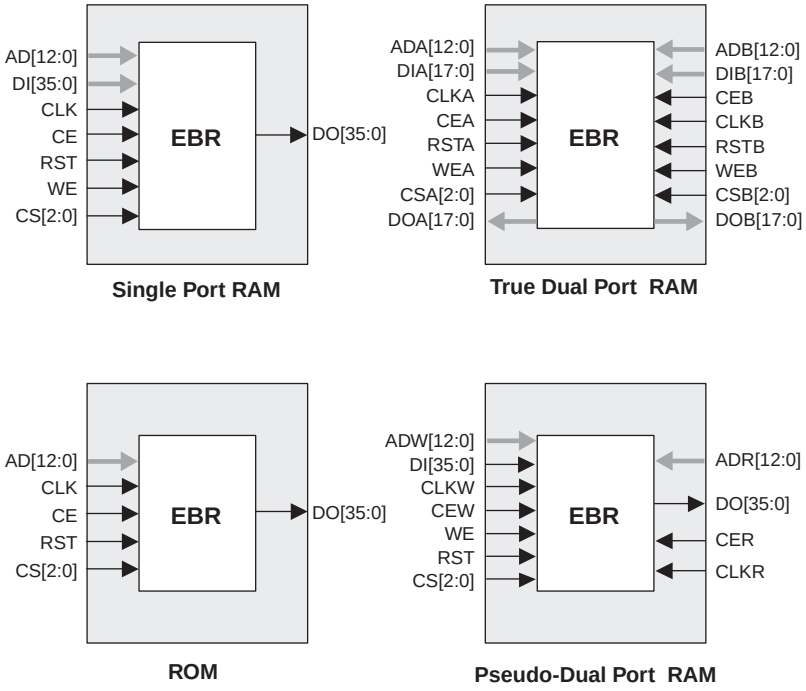
Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-11 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-11. sysMEM EBR Primitives



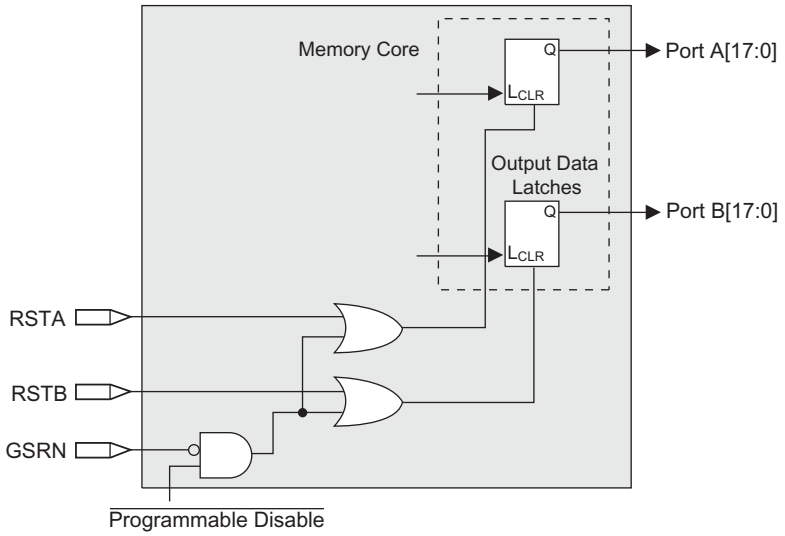
The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output.
2. **Write Through** – a copy of the input data appears at the output of the same port, during a write cycle.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-12.

Figure 2-12. Memory Core Reset



For further information on sysMEM EBR block, please see the details of additional technical documentation at the end of this data sheet.

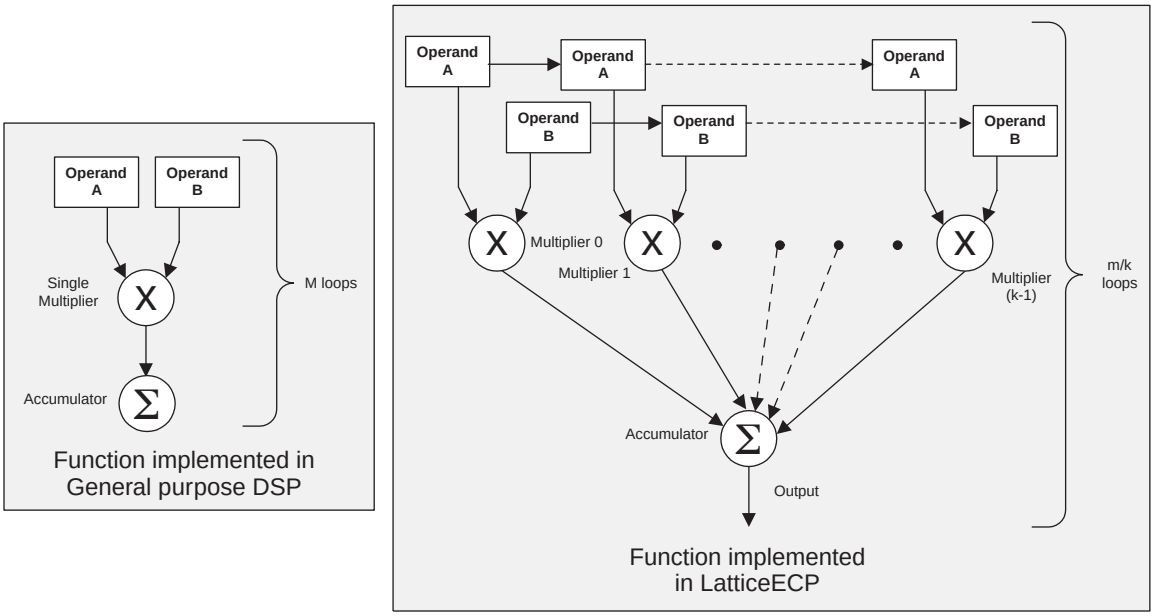
sysDSP Block

The LatticeECP-DSP family provides a sysDSP block making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters; Fast Fourier Transforms (FFT) functions, correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compare to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing appropriate level of parallelism. Figure 2-13 compares the serial and the parallel implementations.

Figure 2-13. Comparison of General DSP and LatticeECP-DSP Approaches



sysDSP Block Capabilities

The sysDSP block in the LatticeECP-DSP family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP-DSP family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block.

The resources in each sysDSP block can be configured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADD (Multiply, Addition/Subtraction)
- MULTADDSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends in the width selected from the three available options x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-1 shows the capabilities of the block.

Table 2-7. Maximum Number of Elements in a Block

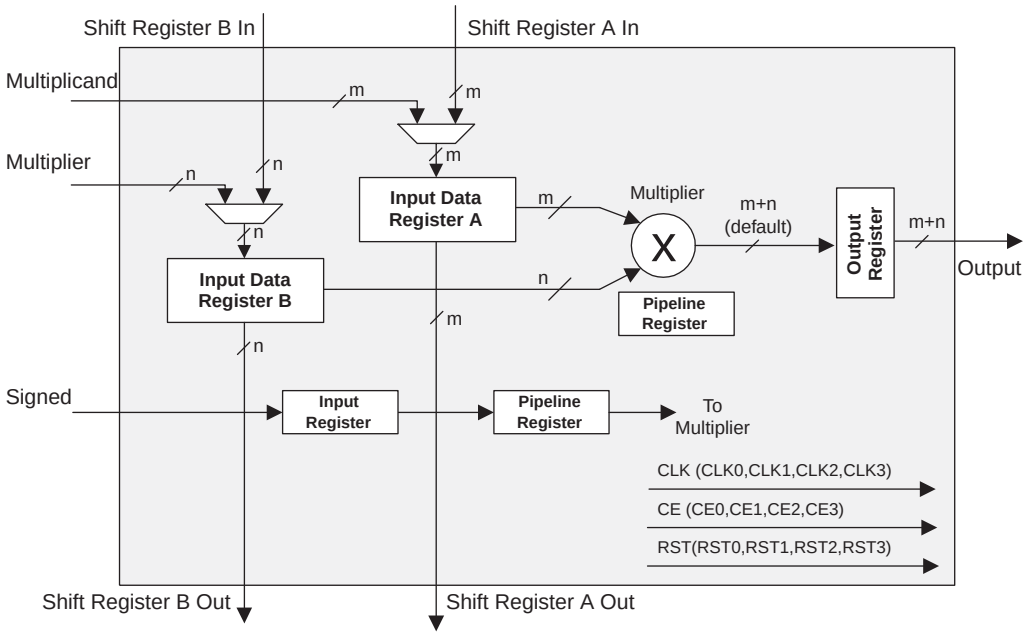
Width of Multiply	x9	x18	x36
MULT	8	4	1
MAC	2	1	—
MULTADD	4	2	—
MULTADDSUM	4	2	—

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift register from previous operand registers. In addition by selecting ‘dynamic operation’ in the ‘Signed/Unsigned’ options the operands can be switched between signed and unsigned on every cycle. Similarly by selecting ‘Dynamic operation’ in the ‘Add/Sub’ option the Accumulator can be switched between addition and subtraction on every cycle.

MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-14 shows the MULT sysDSP element.

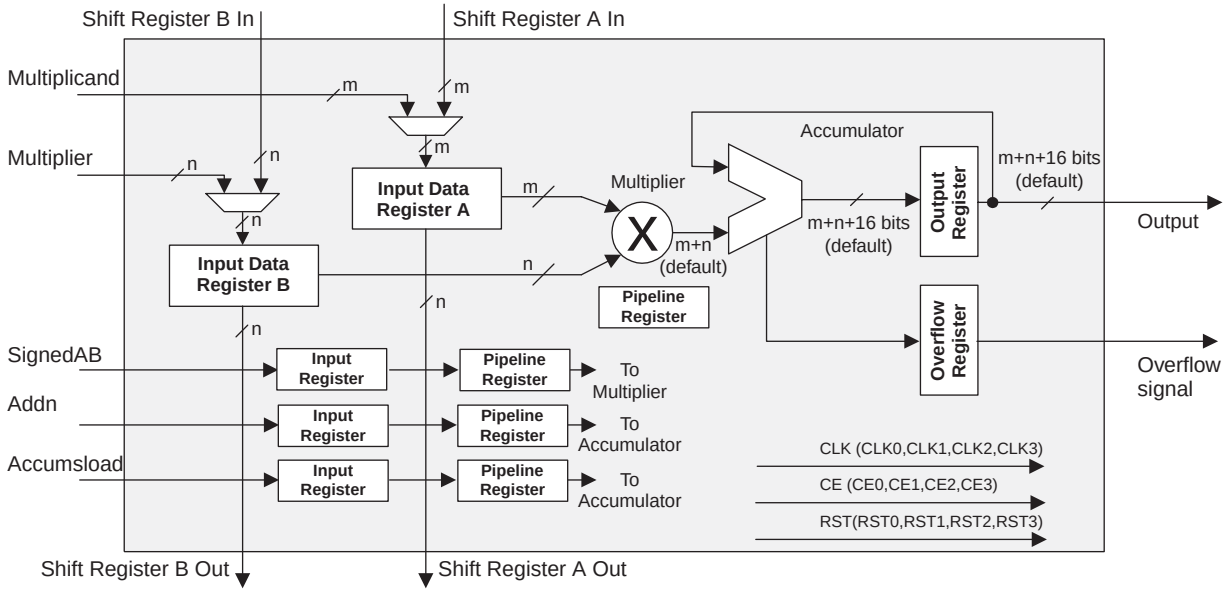
Figure 2-14. MULT sysDSP Element



MAC sysDSP Element

In this case the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-15 shows the MAC sysDSP element.

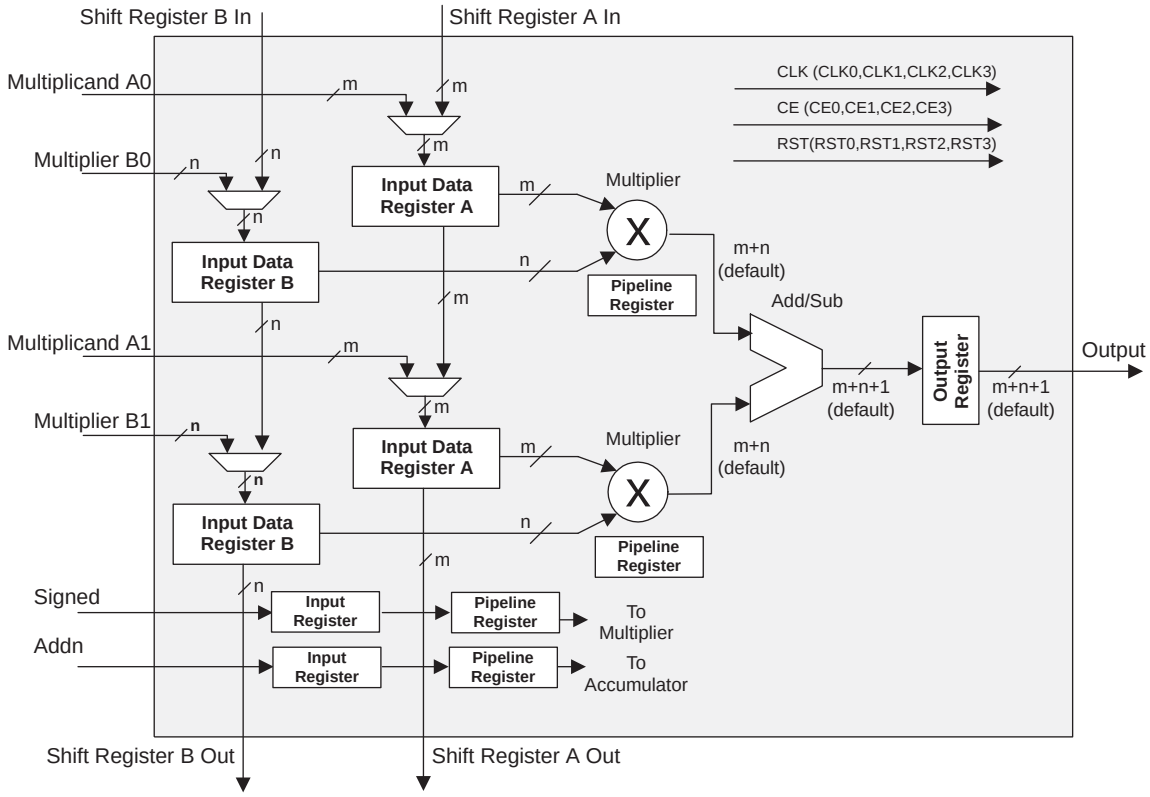
Figure 2-15. MAC sysDSP Element



MULTADD sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-16 shows the MULTADD sysDSP element.

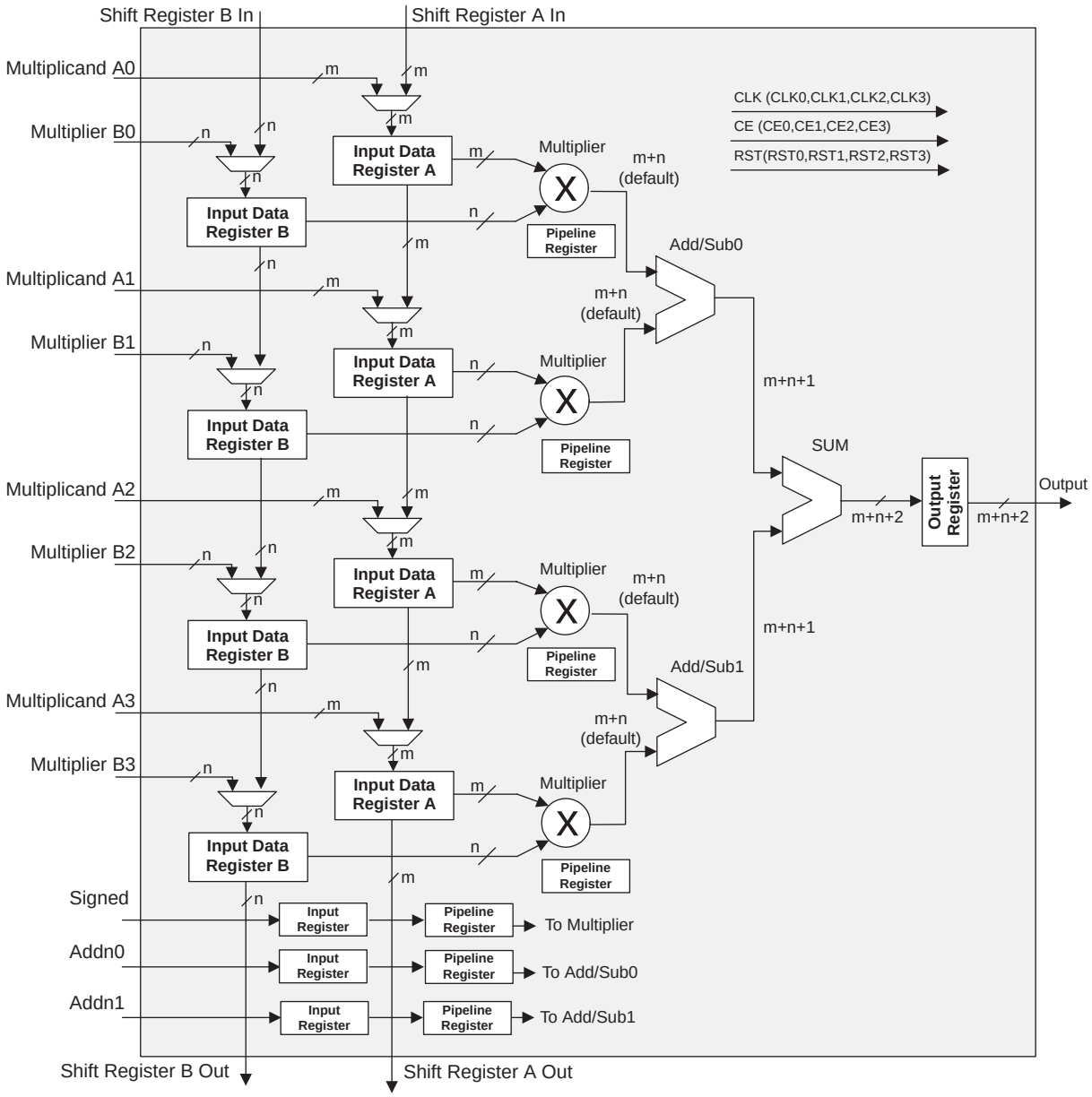
Figure 2-16. MULTADD



MULTADDSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-17 shows the MULTADDSUM sysDSP element.

Figure 2-17. MULTADDSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock enable (CE) and

Reset (RST) are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

Signed and Unsigned with Different Widths

The DSP block supports different widths of signed and unsigned multipliers besides x9, x18 and x36 widths. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-8 provides an example of this.

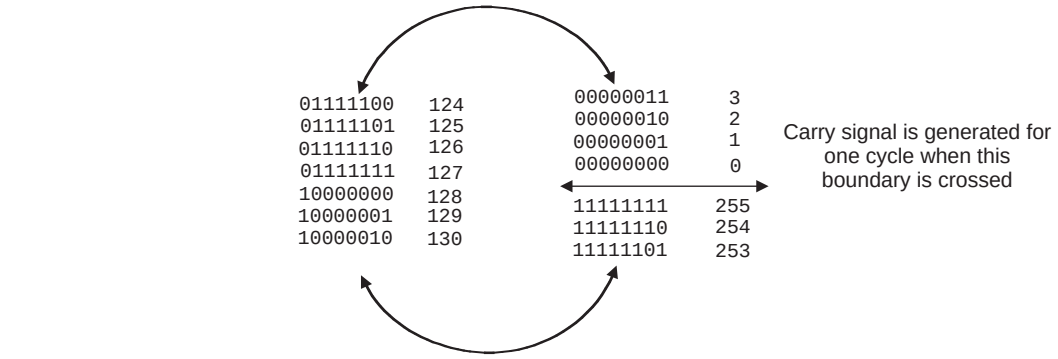
Table 2-8. An Example of Sign Extension

Number	Unsigned	Unsigned 9-bit	Unsigned 18-bit	Signed	Two's Complement Signed 9-Bits	Two's Complement Signed 18-bits
+5	0101	00000101	00000000 00000101	0101	00000101	00000000 00000101
-6	0110	00000110	00000000 00000110	1010	11111010	11111111 11111010

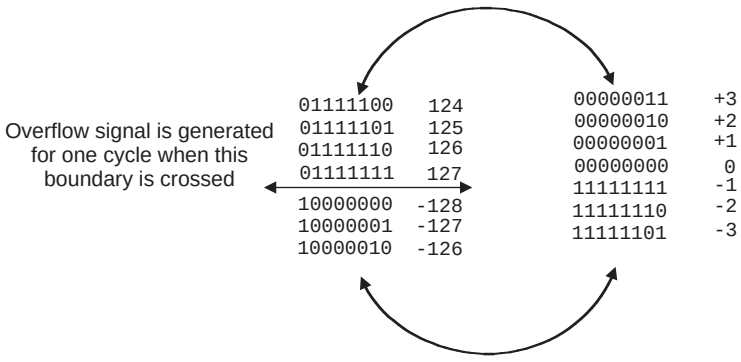
OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. When two unsigned numbers are added and the result is a smaller number then accumulator roll over is said to occur and overflow signal is indicated. When two positive numbers are added with a negative sum and when two negative numbers are added with a positive sum, then the accumulator "roll-over" is said to have occurred and an overflow signal is indicated. Note when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions overflow signal for signed and unsigned operands are listed in Figure 2-18.

Figure 2-18. Accumulator Overflow/Underflow Conditions



Unsigned Operation



Signed Operation

ispLEVER Module Manager

The user can access the sysDSP block via the ispLEVER Module Manager, which has options to configure each DSP module (or group of modules) or through direct HDL instantiation. Additionally Lattice has partnered Mathworks to support instantiation in the Simulink tool, which is a Graphical Simulation Environment. Simulink works with ispLEVER and dramatically shortens the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IPs planned for LatticeECP DSP are: Bit Correlators, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/ Decoder, Turbo Encoder/Decoders and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IPs.

Resources Available in the LatticeECP Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP family. Table 2-10 shows the maximum available EBR RAM Blocks in each of the LatticeECP family. EBR blocks, together with Distributed RAM can be used to store variables locally for the fast DSP operations.

Table 2-9. Number of DSP Blocks in LatticeECP Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
LFECP6	4	32	16	4
LFECP10	5	40	20	5
LFECP15	6	48	24	6
LFECP20	7	56	28	7
LFECP40	10	80	40	10

Table 2-10. Embedded SRAM in LatticeECP family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
LFECP6	10	92
LFECP10	30	276
LFECP15	38	350
LFECP20	46	424
LFECP40	70	645

DSP Performance of the LatticeECP Family

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP family.

Table 2-11. DSP Block performance of LatticeECP Family

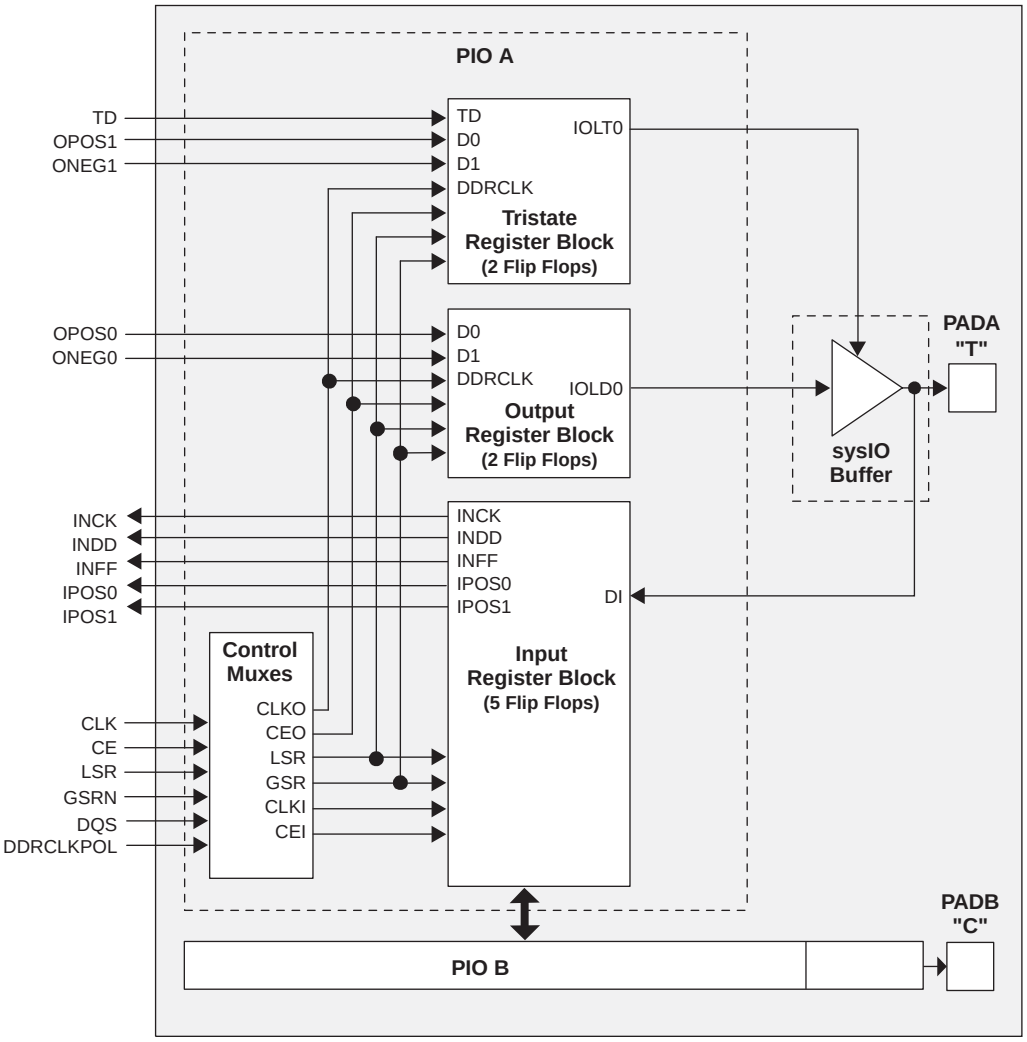
Device	DSP Block	DSP Performance MMAC
LFECP6	4	
LFECP10	5	
LFECP15	6	
LFECP20	7	
LFECP40	10	

For further information on the sysDSP block, please see details of additional technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO Buffers which are then connected to the PADs as shown in Figure 2-19. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysIO buffer, and receives input from the buffer.

Figure 2-19. PIC Diagram



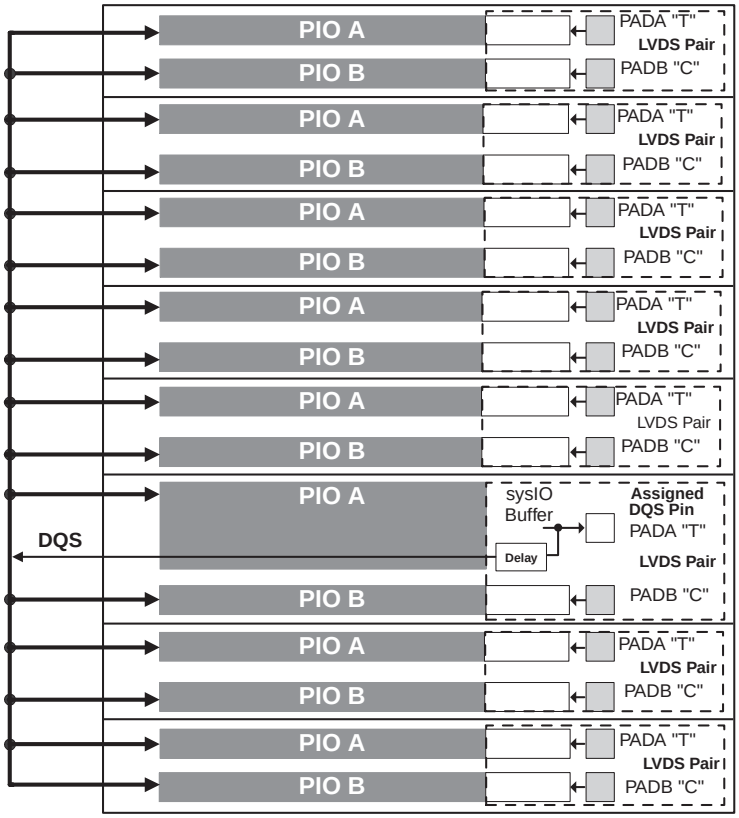
Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-20. The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

Table 2-12. PIO Signal List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block FFs.
CLK0, CLK1	Control from the core	System clocks for input and output blocks.
LSR	Control from the core	Local Set/Reset.
GSRN	Control from routing	Global Set/Reset (active low).
INCK	Input to the core	Input to Primary Clock Network or PLL reference inputs.
DQS	Input to PIO	DQS signal from logic (routing) to PIO.
INDD	Input to the core	Unregistered data input to core.
INFF	Input to the core	Registered input on positive edge of the clock (CLK0).
IPOS0, IPOS1	Input to the core	DDRX registered inputs to the core.
ONEG0	Control from the core	Output signals from the core for SDR and DDR operation.
OPOS0,	Control from the core	Output signals from the core for DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation.
TD	Tristate control from the core	Tristate signal from the core used in SDR operation.
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block.

Figure 2-20. DQS Routing



PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-21 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, reduces input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-22 shows the input register waveforms for DDR operation and Figure 2-23 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-21. Input Register Diagram

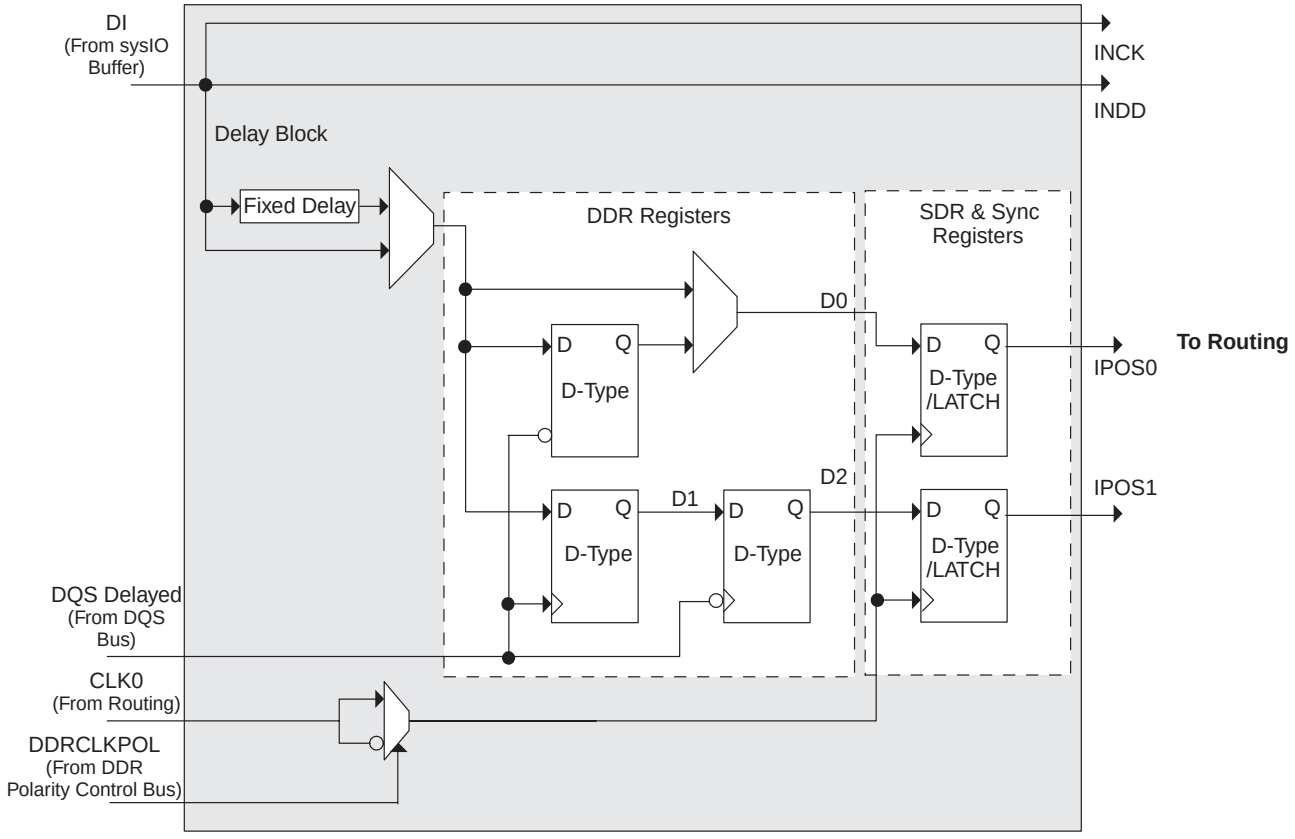


Figure 2-22. Input Register DDR Waveforms

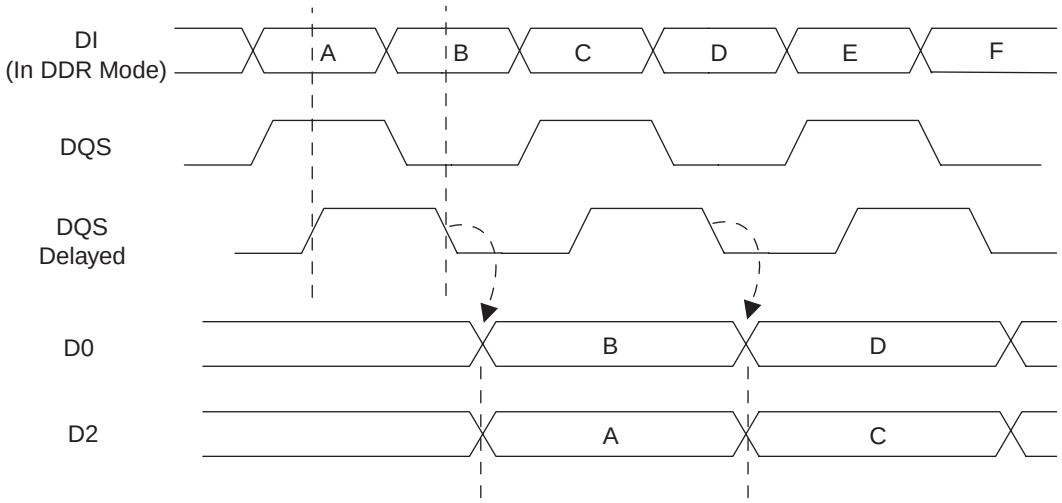
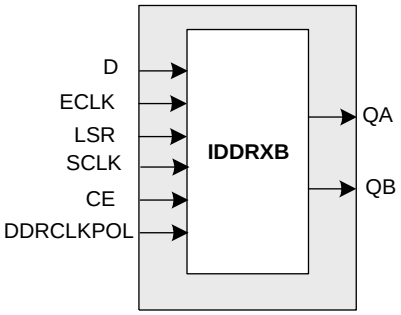


Figure 2-23. INDDRXB Primative



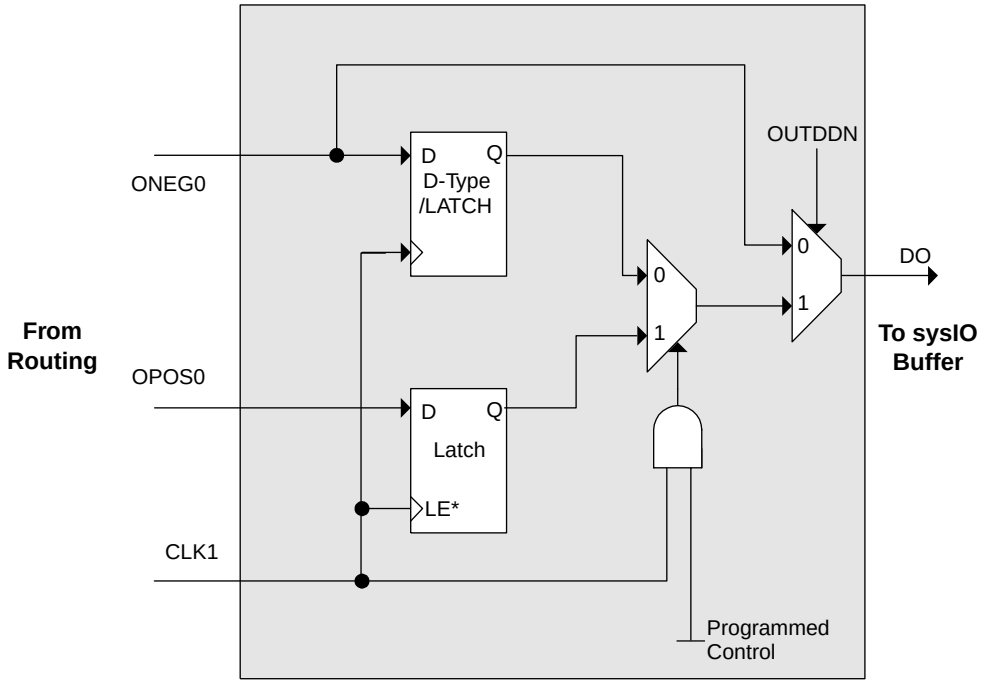
Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-24 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

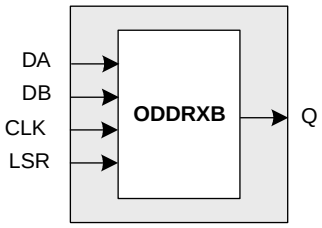
Figure 2-25 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-24. Output Register Block



*Latch is transparent when input is low.

Figure 2-25. ODDRXB Primative

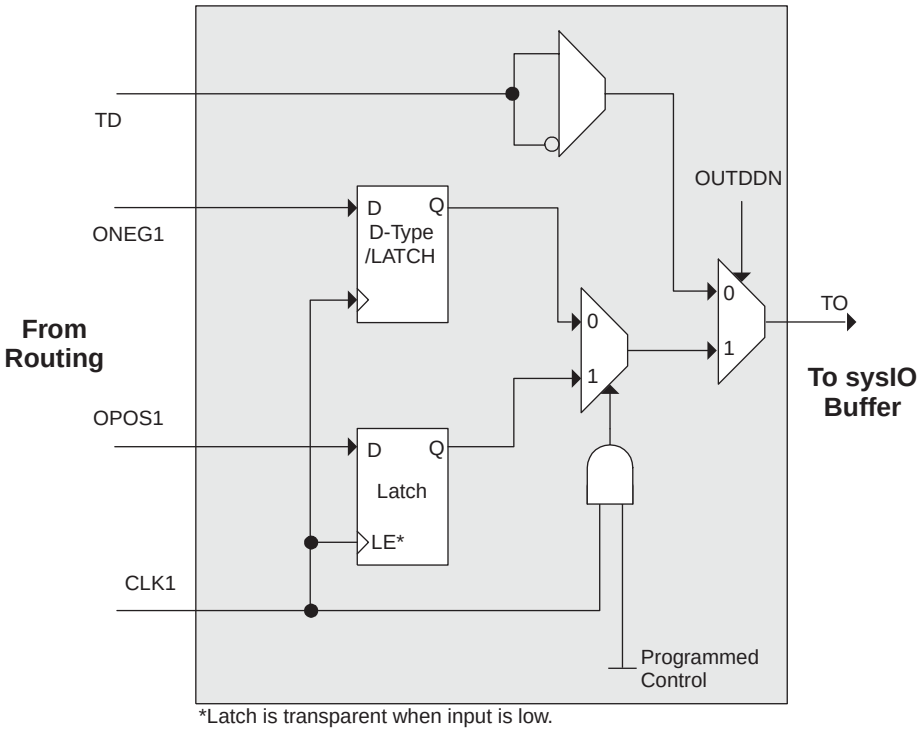


Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-26 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-26. Tristate Register Block



*Latch is transparent when input is low.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the EC devices provide this capability. In addition to these registers, the EC devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment, however in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-27 and 2-28 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-28. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Figure 2-27. DQS Local Bus.

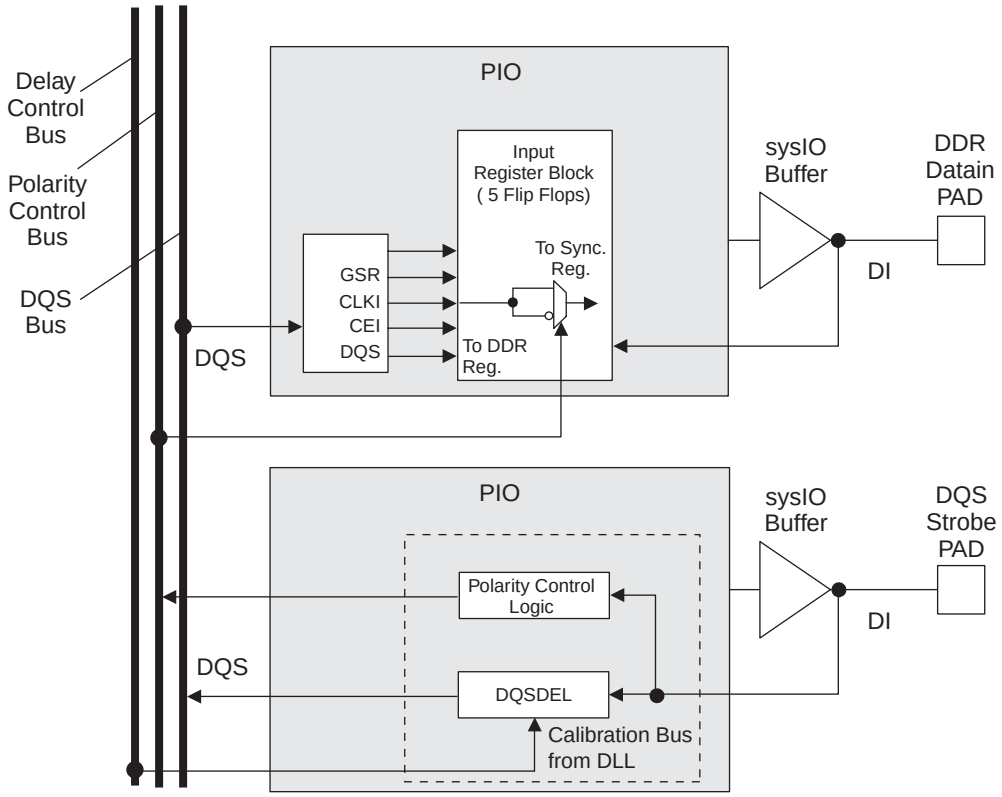
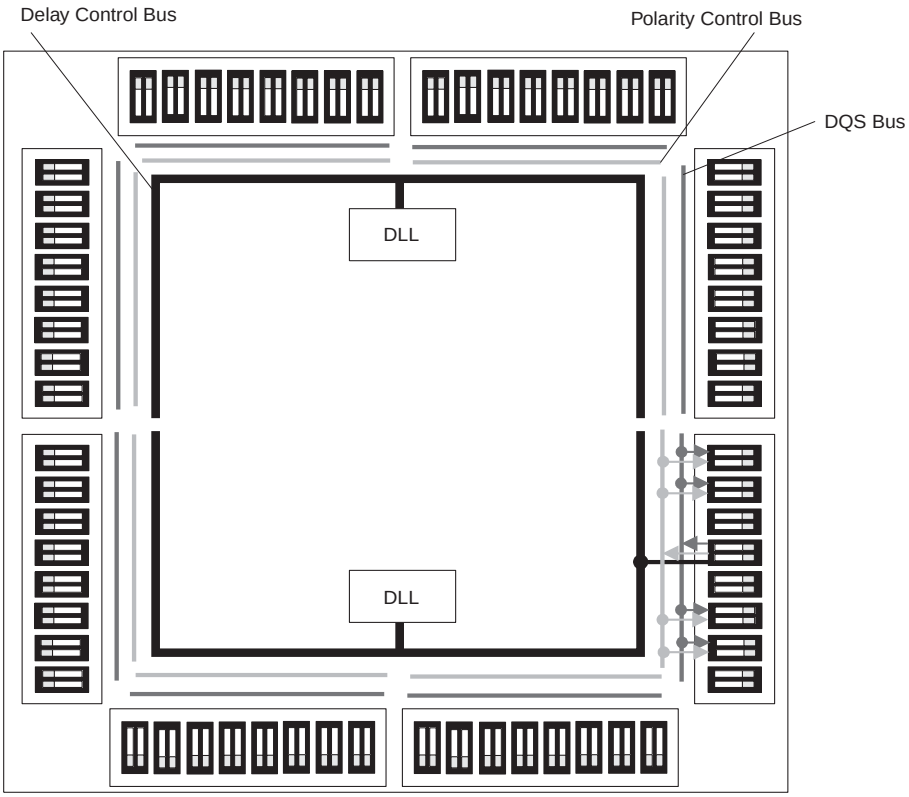


Figure 2-28. DLL Calibration Bus and DQS/DQS Transition Distribution



Polarity Control Logic

In a typical DDR Memory interface design, the phase relation between the incoming delayed DQS strobe and the internal system Clock (during the READ cycle) is unknown.

The LatticeECP/EC family contains dedicated circuits to transfer data between these domains. To prevent setup and hold violations at the domain transfer between DQS (delayed) and the system Clock a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in eight groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

sysIO Buffer Banks

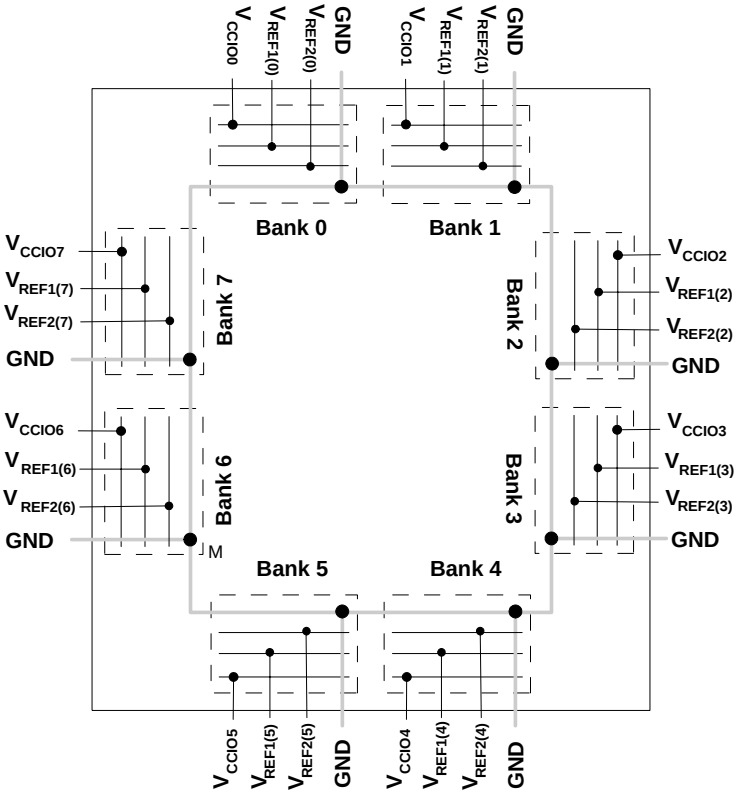
LatticeECP/EC devices have eight sysIO buffer banks; each is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-29 shows the eight banks and their associated supplies.

In the LatticeECP/EC devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI and PCI-X) are powered using $V_{CCIO.}$ LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold

input independent of $V_{CCIO.}$ In addition to the bank V_{CCIO} supplies, the LatticeECP/EC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeECP/EC devices, some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-29. LatticeECP/EC Banks



Note: N and M are the maximum number of I/Os per bank.

LatticeECP/EC devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pair (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on the top and bottom banks have PCI clamp.

2. **Left and Right sysIO Buffer Pair (Differential and Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   Only the left and right banks have LVDS differential output drivers.

Supported Standards

The LatticeECP/EC sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/O standards (together with their supply and reference voltages) supported by the LatticeECP/EC devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical information at the end of this data sheet.

Table 2-13. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)
Single Ended Interfaces		
LVTTL	—	—
LVCMOS33[2]	—	—
LVCMOS25[2]	—	—
LVCMOS18	—	1.8
LVCMOS15	—	1.5
LVCMOS12[2]	—	—
PCI	—	3.3
HSTL18 Class I, II	0.9	—
HSTL18 Class III	1.08	—
HSTL15 Class I	0.75	—
HSTL15 Class III	0.9	—
SSTL3 Class I, II	1.5	—
SSTL2 Class I, II	1.25	—
SSTL18 Class I	0.9	—
Differential Interfaces		
Differential SSTL18 Class I	—	—
Differential SSTL2 Class I, II	—	—
Differential SSTL3 Class I, II	—	—
Differential HSTL15 Class I, III	—	—
Differential HSTL18 Class I, II, III	—	—
LVDS, LVPECL	—	—
BLVDS	—	—

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.
2. JTAG inputs do not have a fixed threshold option and always follow V_{CCJ}.

Table 2-14. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3

1. Emulated with external resistors.

Hot Socketing

The LatticeECP/EC devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, this allows for easy integration with the rest of the system. These capabilities make the LatticeECP/EC ideal for many multiple power supply and hot-swap applications.

Configuration and Testing

The following section describes the configuration and testing features of the LatticeECP/EC family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP/EC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

Device Configuration

All LatticeECP/EC devices contain two possible ports that can be used for device configuration. The test access port (TAP), which supports bit-wide configuration, and the sysCONFIG port that supports both byte-wide and serial configuration.

The TAP supports both the IEEE Std. 1149.1 Boundary Scan specification and the IEEE Std. 1532 In-System Configuration specification. The sysCONFIG port is a 20-pin interface with six of the I/Os used as dedicated pins and the rest being dual-use pins. When sysCONFIG mode is not used, these dual-use pins are available for general purpose I/O. There are four configuration options for LatticeECP/EC devices:

1. Industry standard SPI memories.
2. Industry standard byte wide flash and ispMACH 4000 for control/addressing.
3. Configuration from system microprocessor via the configuration bus or TAP.
4. Industry standard FPGA board memory.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port. Once a configuration port is selected, that port is locked and another configuration port cannot be activated until the next power-up sequence.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Internal Logic Analyzer Capability (ispTRACY)

All LatticeECP/EC devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time.

For more information on ispTRACY, please see information regarding additional technical documentation at the end of this data sheet.

External Resistor

LatticeECP/EC devices require a single external, 10K ohm +/- 1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

Oscillator

Every LatticeECP/EC device has an internal CMOS oscillator which is used to derive a master serial clock for configuration. The oscillator and the master serial clock run continuously. The default value of the master serial clock is 2.5MHz. Table 2-15 lists all the available Master Serial Clock frequencies. When a different Master Serial Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Serial Clock frequency.
2. During configuration the device starts with the default (2.5MHz) Master Serial Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Serial Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information on the use of this oscillator for configuration, please see details of additional technical documentation at the end of this data sheet.

Table 2-15. Selectable Master Serial Clock (CCLK) Frequencies During Configuration

CCLK (MHz)	CCLK (MHz)	CCLK (MHz)
2.5*	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—
10.0	41	—

Density Shifting

The LatticeECP/EC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

LatticeECP/EC Family Data Sheet DC and Switching Characteristics

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . -0.5 to 1.32V

Supply Voltage V_{CCAUX} . . . . . -0.5 to 3.75V

Supply Voltage V_{CCJ} . . . . . -0.5 to 3.75V

Output Supply Voltage V_{CCIO} . . . . . -0.5 to 3.75V

Input Voltage Applied[4] . . . . . -0.5 to 4.25V

I/O Tristate Voltage Applied [4] . . . . . -0.5 to 3.75V

Storage Temperature (Ambient) . . . . . -65 to 150°C

Junction Temp. (Tj) +125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCIO}[1, 2]	I/O Driver Supply Voltage	1.140	3.465	V
V_{CCJ}[1]	Supply Voltage for IEEE 1149.1 Test Access Port	1.140	3.465	V
t_{JCOM}	Junction Commercial Operation	0	+85	°C
t_{JIND}	Junction Industrial Operation	-40	100	°C

1. If V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}.
2. See recommended voltages by I/O standard in subsequent table.

Hot Socketing Specifications[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Input or I/O leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	+/-1000	µA

1. Insensitive to sequence of V_{CC}, V_{CCAUX} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX} and V_{CCIO}.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
4. LVCMOS and LVTTL only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low leakage	$0 \le V_{IN} \le (V_{CCIO} - 0.2V)$	—	—	10	µA
		$(V_{CCIO} - 0.2V) \le V_{IN} \le 3.6V$	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	30	—	150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	-30	—	-150	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHLH}	Bus Hold High Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz

Supply Current (Standby)[1, 2, 3]

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Typ.	Max.	Units
I_{CC}	Core Power Supply Current	LFEC1			mA
		LFEC3			mA
		LFEC6/LFECP6			mA
		LFEC10/LFECP10			mA
		LFEC15/LFECP15			mA
		LFEC20/LFECP20	60		mA
		LFEC40/LFECP40			mA
I_{CCAUX}	Auxiliary Power Supply Current	LFEC1			mA
		LFEC3			mA
		LFEC6/LFECP6			mA
		LFEC10/LFECP10			mA
		LFEC15/LFECP15			mA
		LFEC20/LFECP20	15		mA
		LFEC40/LFECP40			mA
I_{CCPLL}	PLL Power Supply	LFEC1, LFEC3, LFEC6, LFECP6			mA
		LFEC10, LFEC15, LFEC20, LFEC40, LFECP10, LFECP15, LFECP20, LFECP40			mA
I_{CCIO}	Bank Power Supply Current		15		mA
I_{CCJ}	V_{CCJ} Power Supply Current		1		mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.

Initialization Supply Current[1]

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Typ.	Max.	Units
I_{CC}	Core Power Supply Current	LFEC1			mA
		LFEC3			mA
		LFEC6/LFECP6			mA
		LFEC10/LFECP10			mA
		LFEC15/LFECP15			mA
		LFEC20/LFECP20			mA
		LFEC40/LFECP40			mA
I_{CCAUX}	Auxiliary Power Supply Current	LFEC1			mA
		LFEC3			mA
		LFEC6/LFECP6			mA
		LFEC10/LFECP10			mA
		LFEC15/LFECP15			mA
		LFEC20/LFECP20			mA
		LFEC40/LFECP40			mA
I_{CCPLL}	PLL Power Supply	LFEC1, LFEC3, LFEC6, LFECP6			mA
		LFEC10, LFEC15, LFEC20, LFEC40, LFECP10, LFECP15, LFECP20, LFECP40			mA
I_{CCIO}	Bank Power Supply Current				mA
I_{CCJ}	V_{CCJ} Power Supply Current				mA

1. Until DONE signal is active.

sysIO Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18 Class I	1.71	2.5	1.89	1.15	1.25	1.35
SSTL2 Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15 Class III	1.425	1.5	1.575	—	0.9	—
HSTL 18 Class I, II	1.71	1.8	1.89	—	0.9	—
HSTL 18 Class III	1.71	1.8	1.89	—	1.08	—
LVDS	2.375	2.5	3.625	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resisters.

sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
SSTL18 class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
HSTL15 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
HSTL15 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8
HSTL18 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	9.6	-9.6
HSTL18 class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16
HSTL18 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

sysIO Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input voltage		0	—	2.4	V
V_{THD}	Differential input threshold		+/-100	—	—	mV
V_{CM}	Input common mode voltage	100mV ≤ V_{THD}	V_{THD}/2	1.2	1.8	V
		200mV ≤ V_{THD}	V_{THD}/2	1.2	1.9	V
		350mV ≤ V_{THD}	V_{THD}/2	1.2	2.0	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	6	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

BLVDS

The LatticeECP/EC devices support BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-1 is one possible solution for bi-directional multi-point differential signals.

Figure 3-1. BLVDS Multi-point Output Example

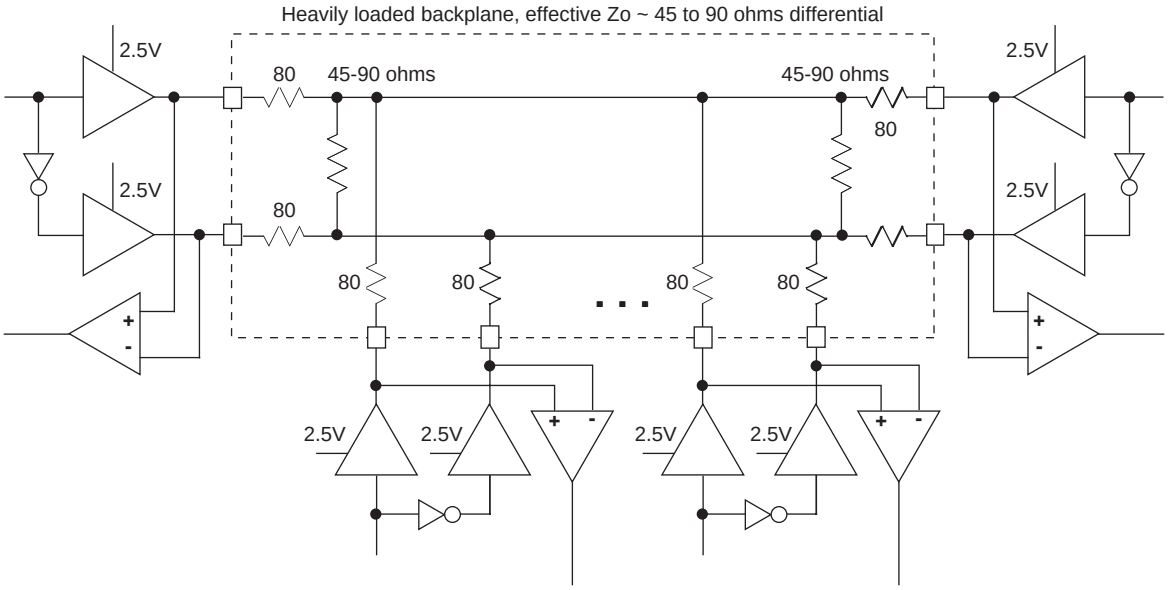


Table 3-1. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	ohm
R_{TLEFT}	Left end termination	45	90	ohm
R_{TRIGHT}	Right end termination	45	90	ohm
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LVPECL

The LatticeECP/EC devices support differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-2 is one possible solution for point-to-point signals.

Figure 3-2. Differential LVPECL

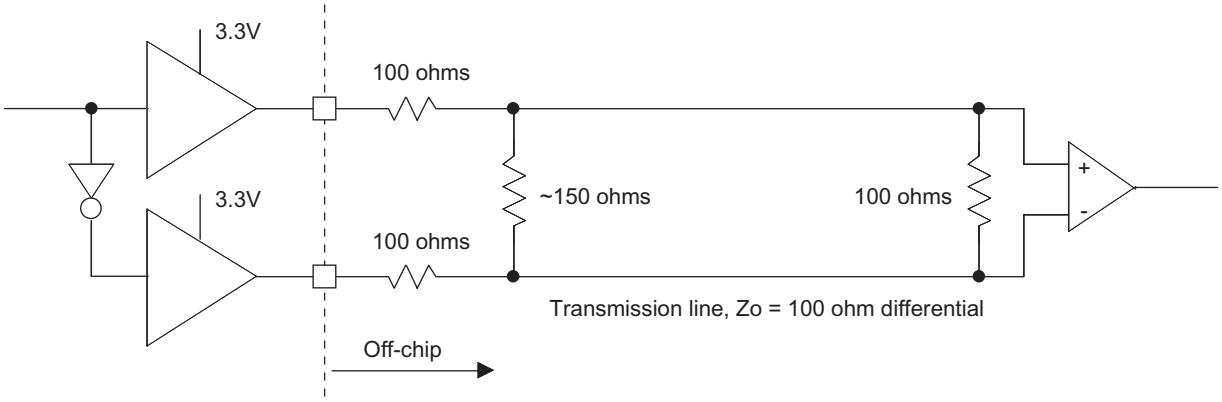


Table 3-2. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	100	ohm
R_P	Driver parallel resistor	150	ohm
R_T	Receiver termination	100	ohm
V_{OH}	Output high voltage	2.03	V
V_{OL}	Output low voltage	1.27	V
V_{OD}	Output differential voltage	0.76	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	85.7	ohm
I_{DC}	DC output current	12.7	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical information at the end of this data sheet.

RSDS

The LatticeECP/EC devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-3 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-3 are industry standard values for 1% resistors.

Figure 3-3. RSDS (Reduced Swing Differential Standard)

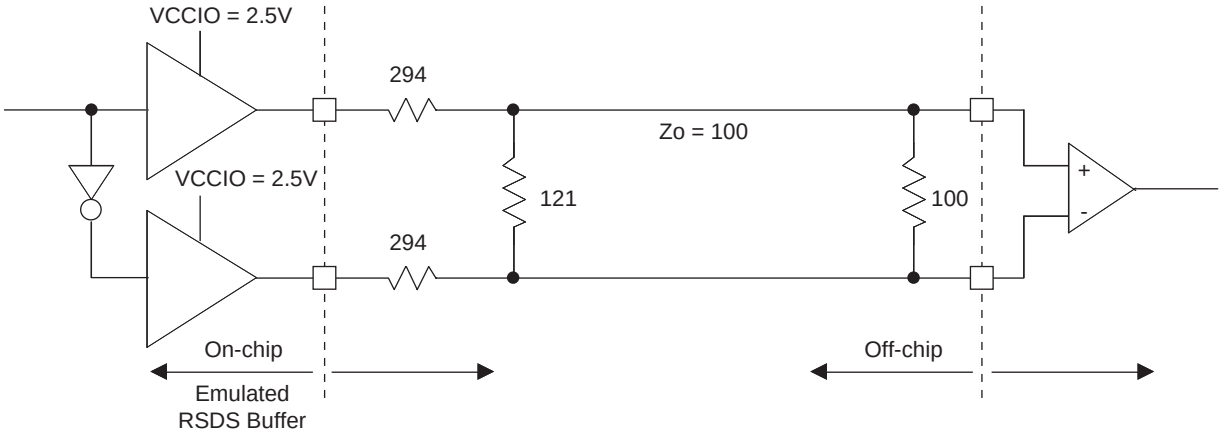


Table 3-3. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance		ohm
R_S	Driver series resistor		ohm
R_P	Driver parallel resistor		ohm
R_T	Receiver termination		ohm
V_{OH}	Output high voltage		V
V_{OL}	Output low voltage		V
V_{OD}	Output differential voltage		V
V_{CM}	Output common mode voltage		V
Z_{BACK}	Back impedance		ohm
I_{DC}	DC output current		mA

5V Tolerant Input Buffer

The input buffers of the LatticeECP/EC family of devices can support 5V signals by using a PCI Clamp and an external series resistor as shown in Figure 3-4. A suitable resistor can be selected by using the PCI Clamp Characteristic as shown in Figure 3-5.

Figure 3-4. 5 V Tolerant Input Buffer

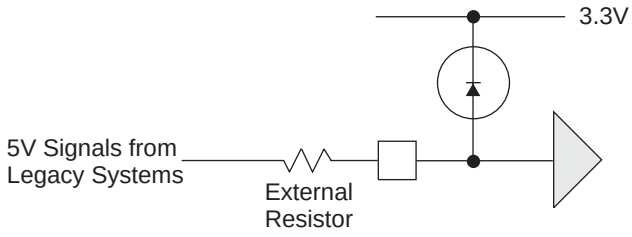
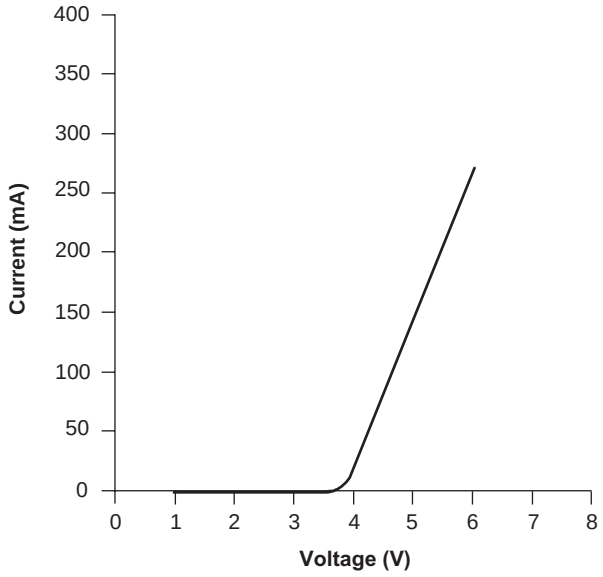


Figure 3-5. Typical PCI Clamp Current



Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	6.8	ns
32-bit decoder	7.8	ns
64-bit decoder	8.4	ns
4:1 MUX	5.7	ns
8:1 MUX	5.9	ns
16:1 MUX	6.5	ns
32:1 MUX	6.9	ns
Combinatorial (pin to LUT to pin)	5.3	ns
Embedded Memory Functions		
Pin to EBR input register setup	0.0	ns
EBR output clock to pin	11.3	ns
Distributed PFU RAM		
Pin to PFU RAM register setup	0.0	ns
PFU RAM clock to pin	6.8	ns

Register-to-Register Performance

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	263	MHz
32-bit decoder	230	MHz
64-bit decoder	211	MHz
4:1 MUX	500	MHz
8:1 MUX	375	MHz
16:1 MUX	360	MHz
32:1 MUX	373	MHz
8-bit adder	314	MHz
16-bit adder	251	MHz
64-bit adder	146	MHz
16-bit counter	360	MHz
32-bit counter	280	MHz
64-bit counter	180	MHz
64-bit accumulator	125	MHz
Embedded Memory Functions		
256x36 Single Port RAM	305	MHz
512x18 True-Dual Port RAM	308	MHz
Distributed Memory Functions		
16x2 Single Port RAM	455	MHz
64x2 Single Port RAM	244	MHz
128x4 Single Port RAM	196	MHz
32x2 Pseudo-Dual Port RAM	341	MHz
64x4 Pseudo-Dual Port RAM	303	MHz

Register-to-Register Performance (Continued)

Function	-5 Timing	Units
DSP Function		
9x9 Pipelined Multiply/Accumulate[1]	265	MHz
18x18 Pipelined Multiply/Accumulate[1]	226	MHz
36x36 Pipelined Multiply[1]	177	MHz

1. Applies to LatticeECP devices only.

Derating Timing Tables

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst-case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process, can be much better than the values given in the tables. To calculate logic timing numbers at a particular temperature and voltage multiply the noted numbers with the derating factors provided below.

The junction temperature for the FPGA depends on the power dissipation by the device, the package thermal characteristics (Θ_{JA}), and the ambient temperature, as calculated with the following equation:

$$T_{JMAX} = T_{AMAX} + (Power * \Theta_{JA})$$

The user must determine this temperature and then use it to determine the derating factor based on the following derating tables: T_J °C.

Table 3-4. Delay Derating Table for Internal Blocks

T_J °C Commercial	T_J °C Industrial	Power Supply Voltage		
		1.14V	1.2V	1.26V
—	-40			
—	-25			
0	15			
25	40			
85	100			
100	115			
110	125			
125	—			

LatticeECP/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Primary Clock without PLL)[1]									
t_{CO}	Clock to Output - PIO Output Register	LFEC20	—	6.75	-	8.43	—	11.25	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LFEC20	0.00	—	0.00	—	0.00	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	LFEC20	2.55	—	3.19	—	4.25	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with data input delay	LFEC20	2.85	—	3.42	—	3.99	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFEC20	0.00	—	0.00	—	0.00	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LFEC20	—		—		—		Mhz
DDR I/O Pin Parameters[2]									
t_{DVBDQ}	Data Valid Before DQS (DDR Read)	LFEC20	—		—		—		ps
t_{DVADQ}	Data Valid After DQS (DDR Read)	LFEC20		—		—		—	ps
t_{DQ_SK}	Data Skew (DDR Write)	LFEC20	—		—		—		ps
t_{DQS_JIT}	DQS Jitter (DDR Write)	LFEC20	—		—		—		ps
f_{MAX_DDR}	DDR Clock Frequency	LFEC20	—	166	—		—		MHz

1. General timing numbers based on LVCMOS2.5V, 12 mA.
2. DDR timing numbers based on SSTL I/O.

LatticeECP/EC Internal Timing Parameters[1]

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.25	—	0.31	—	0.36	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.55	—	0.66	—	0.77	ns
t_{LSR_PFU}	Set/Reset to output of PFU	—	0.81	—	0.98	—	1.14	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) input setup time	0.08	—	0.10	—	0.11	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) input hold time	-0.06	—	-0.07	—	-0.08	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.09	—	0.10	—	0.12	—	ns
t_{HD_PFU}	Clock to D input hold time	-0.04	—	-0.04	-	-0.05	—	ns
t_{CK2Q_PFU}	Clock to Q delay, D-type register configuration	—	0.43	—	0.51	—	0.60	ns
t_{LE2Q_PFU}	Clock to Q delay latch configuration	—	0.54	—	0.65	—	0.76	ns
t_{LD2Q_PFU}	D to Q throughput delay when latch is enabled	—	0.50	—	0.60	—	0.69	ns
PFU Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output	—	0.43	—	0.51	—	0.60	ns
t_{SUDATA_PFU}	Data Setup Time	-0.25	—	-0.30	—	-0.34	—	ns
t_{HDATA_PFU}	Data Hold Time	-0.06	—	-0.07	—	-0.08	—	ns
t_{SUADDR_PFU}	Address Setup Time	-0.66	—	-0.79	—	-0.92	—	ns
t_{HADDR_PFU}	Address Hold Time	-0.27	—	-0.33	—	-0.38	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	-0.30	—	-0.36	—	-0.42	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	-0.21	—	-0.25	—	-0.29	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay	—		—		—		ns
t_{OUT_PIO}	Output Buffer Delay	—		—		—		ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	—	0.12	—	0.14	—	0.17	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	—	-0.09	—	-0.11	—	-0.13	ns
t_{COO_PIO}	Output Register Clock to Output Delay	—	0.75	—	0.90	—	1.05	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	—	-0.02	—	-0.02	—	-0.03	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	—	0.12	—	0.14	—	0.17	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.10	0.24	0.12	0.29	0.14	0.34	ns
t_{HLSR_PIO}	Set/Reset Hold Time	-0.24	-0.10	-0.29	-0.12	-0.34	-0.14	ns
EBR Timing								
t_{CO_EBR}	Clock to output from Address or Data	—	3.80	—	4.55	—	5.31	ns
t_{COO_EBR}	Clock to output from EBR output Register	—		—		—		ns
tS_{UDATA_EBR}	Setup Data to EBR Memory	-0.34	—	-0.41	—	-0.48	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.37	—	0.44	—	0.52	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	-0.34	—	-0.41	—	-0.48	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.37	—	0.45	—	0.52	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to PFU Memory	-0.22	—	-0.26	—	-0.30	—	ns

LatticeECP/EC Internal Timing Parameters[1] (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.23	—	0.28	—	0.33	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.18	—	0.21	—	0.25	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.17	—	-0.20	—	-0.24	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.47	—	1.76	—	2.05	ns
PLL Parameters								
t_{RSTREC}	Reset Recovery to Rising Clock	—		—		—		ns
t_{RSTSU}	Reset Signal Setup Time	1	—	1	—	1	—	ns
t_{RSTW}	Reset Signal Pulse Width	1.8	—	1.8	—	1.8	—	ns
DSP Block Timing[2]								
t_{SUI_DSP}	Input Register Setup Time	—		—		—		ns
t_{HI_DSP}	Input Register Hold Time	—		—		—		ns
t_{SUP_DSP}	Pipeline Register Setup Time	—		—		—		ns
t_{HP_DSP}	Pipeline Register Hold Time	—		—		—		ns
t_{SUO_DSP}	Output Register Setup Time	—		—		—		ns
t_{HO_DSP}	Output Register Hold Time	—		—		—		ns
t_{COI_DSP}	Input Register Clock to Output Time	—		—		—		ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—		—		—		ns
t_{COO_DSP}	Output Register Clock to Output Time	—		—		—		ns
$t_{COOVRFL\_DSP}$	Overflow Register Clock to Output Time	—		—		—		ns
$t_{SUADSUB}$	AdSub Setup Time	—		—		—		ns
t_{HADSUB}	AdSub Hold Time	—		—		—		ns
t_{SUSIGN}	Sign Setup Time	—		—		—		ns
t_{HSIGN}	Sign Hold Time	—		—		—		ns
$t_{SUACCSLOAD}$	Accumulator Load Setup Time	—		—		—		ns
$t_{HACCSLOAD}$	Accumulator Load Hold Time	—		—		—		ns

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LatticeECP devices only.

Timing Diagrams

PFU Timing Diagrams

Figure 3-6. Slice Single/Dual Port Write Cycle Timing

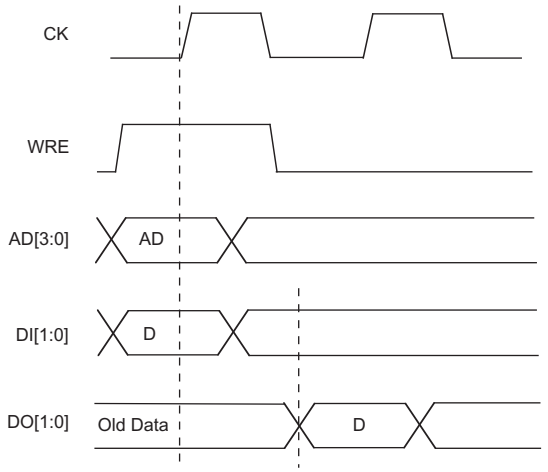
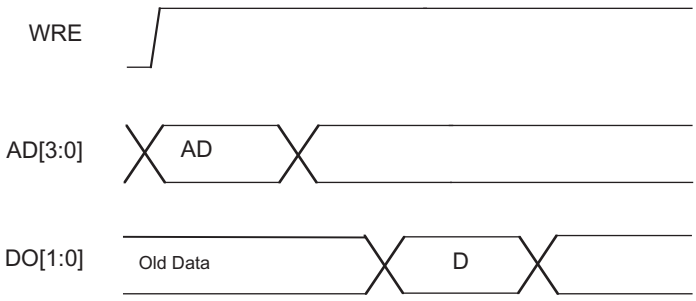
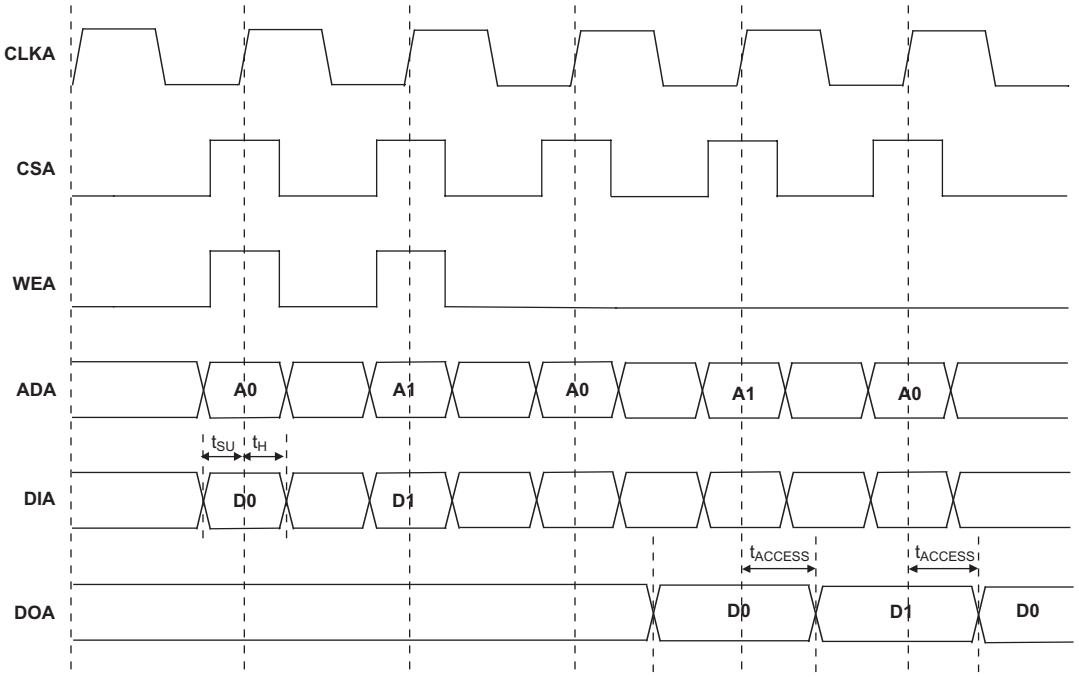


Figure 3-7. Slice Single /Dual Port Read Cycle Timing



EBR Memory Timing Diagrams

Figure 3-8. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-9. Read/Write Mode with Input and Output Registers

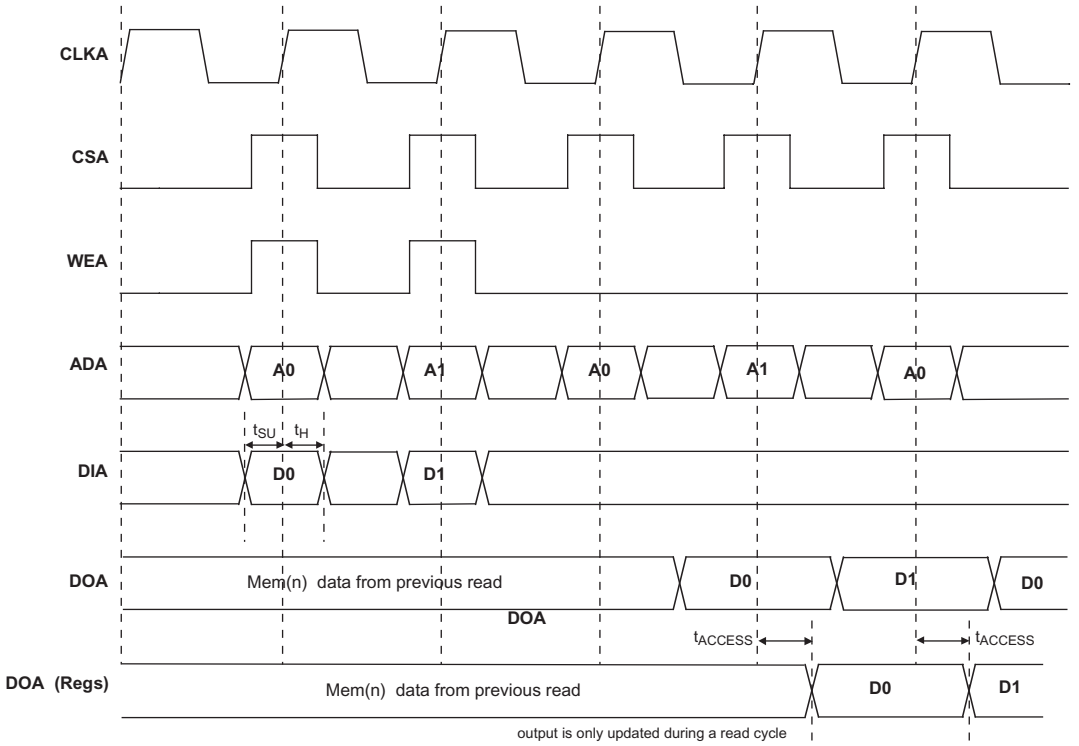
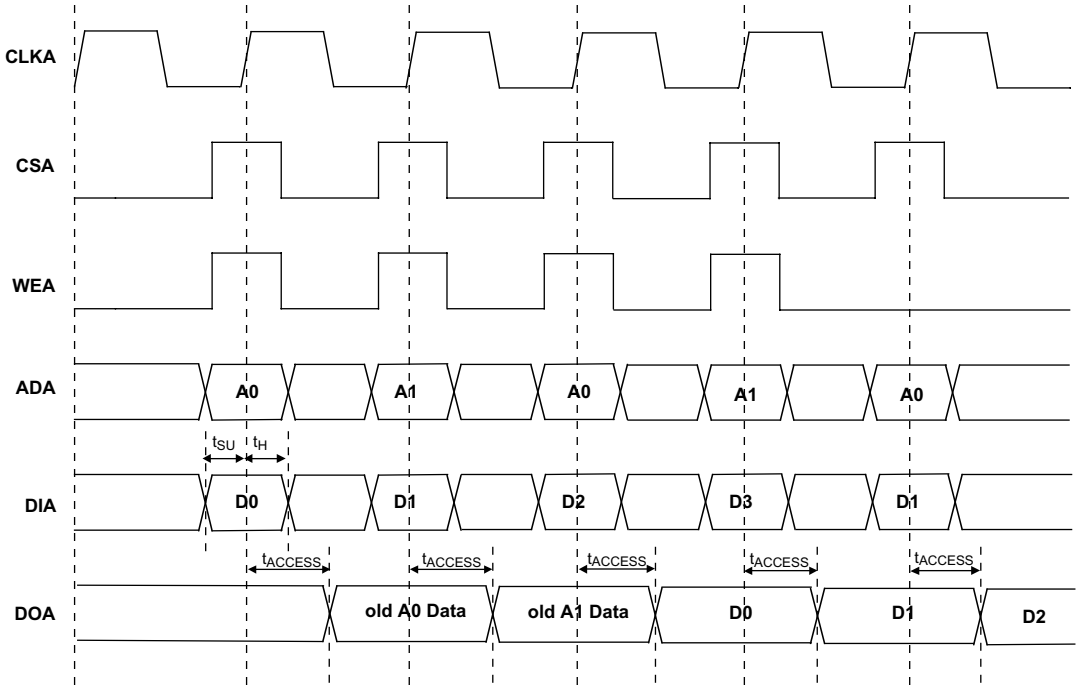
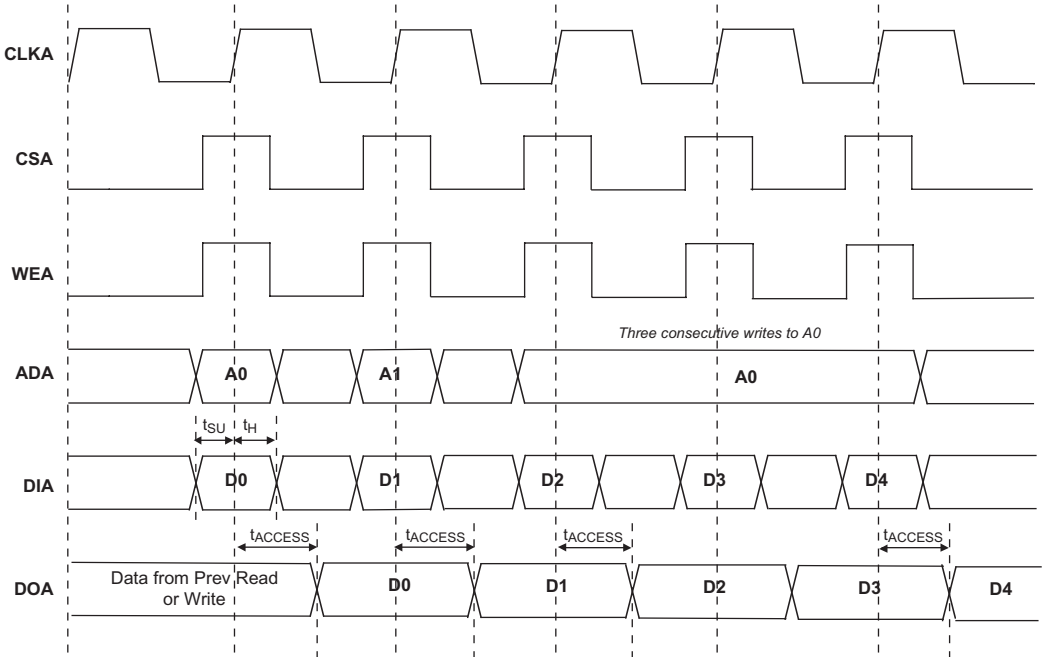


Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LatticeECP/EC Family Timing Adders[1]

Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
Input Adjusters					
LVDS25	LVDS	0.41	0.50	0.58	ns
BLVDS25	BLVDS	0.41	0.50	0.58	ns
LVPECL33	LVPECL	0.50	0.60	0.70	ns
HSTL18_I	HSTL_18 class I	0.41	0.49	0.57	ns
HSTL18_II	HSTL_18 class II	0.41	0.49	0.57	ns
HSTL18_III	HSTL_18 class III	0.41	0.49	0.57	ns
HSTL18D_I	Differential HSTL 18 class I	0.37	0.44	0.52	ns
HSTL18D_II	Differential HSTL 18 class II	0.37	0.44	0.52	ns
HSTL18D_III	Differential HSTL 18 class III	0.37	0.44	0.52	ns
HSTL15_I	HSTL_15 class I	0.40	0.48	0.56	ns
HSTL15_III	HSTL_15 class III	0.40	0.48	0.56	ns
HSTL15D_I	Differential HSTL 15 class I	0.37	0.44	0.51	ns
HSTL15D_III	Differential HSTL 15 class III	0.37	0.44	0.51	ns
SSTL33_I	SSTL_3 class I	0.46	0.55	0.64	ns
SSTL33_II	SSTL_3 class II	0.46	0.55	0.64	ns
SSTL33D_I	Differential SSTL_3 class I	0.39	0.47	0.55	ns
SSTL33D_II	Differential SSTL_3 class II	0.39	0.47	0.55	ns
SSTL25_I	SSTL_2 class I	0.43	0.51	0.60	ns
SSTL25_II	SSTL_2 class II	0.43	0.51	0.60	ns
SSTL25D_I	Differential SSTL_2 class I	0.38	0.45	0.53	ns
SSTL25D_II	Differential SSTL_2 class II	0.38	0.45	0.53	ns
SSTL18_I	SSTL_18 class I	0.40	0.48	0.56	ns
SSTL18D_I	Differential SSTL_18 class I	0.37	0.44	0.51	ns
LVTTL33	LVTTL	0.07	0.09	0.10	ns
LVCMOS33	LVCMOS 3.3	0.07	0.09	0.10	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	0.07	0.09	0.10	ns
LVCMOS15	LVCMOS 1.5	0.24	0.29	0.33	ns
LVCMOS12	LVCMOS 1.2	1.27	1.52	1.77	ns
PCI33	PCI	0.07	0.09	0.10	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E				ns
LVDS25	LVDS 2.5				ns
BLVDS25	BLVDS 2.5				ns
LVPECL33	LVPECL 3.3				ns
HSTL18_I	HSTL_18 class I				ns
HSTL18_II	HSTL_18 class II				ns
HSTL18_III	HSTL_18 class III				ns
HSTL18D_I	Differential HSTL 18 class I				ns
HSTL18D_II	Differential HSTL 18 class II				ns
HSTL18D_III	Differential HSTL 18 class III				ns
HSTL15_I	HSTL_15 class I				ns

LatticeECP/EC Family Timing Adders[1] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
HSTL15_II	HSTL_15 class II				ns
HSTL15_III	HSTL_15 class III				ns
HSTL15D_I	Differential HSTL 15 class I				ns
HSTL15D_III	Differential HSTL 15 class III				ns
SSTL33_I	SSTL_3 class I				ns
SSTL33_II	SSTL_3 class II				ns
SSTL33D_I	Differential SSTL_3 class I				ns
SSTL33D_II	Differential SSTL_3 class II				ns
SSTL25_I	SSTL_2 class I				ns
SSTL25_II	SSTL_2 class II				ns
SSTL25D_I	Differential SSTL_2 class I				ns
SSTL25D_II	Differential SSTL_2 class II				ns
SSTL18_I	SSTL_1.8 class I				ns
SSTL18D_I	Differential SSTL_1.8 class I				ns
LVTTL33_4mA	LVTTL 4mA drive				ns
LVTTL33_8mA	LVTTL 8mA drive				ns
LVTTL33_12mA	LVTTL 12mA drive				ns
LVTTL33_16mA	LVTTL 16mA drive				ns
LVTTL33_20mA	LVTTL 20mA drive				ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive				ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive				ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive				ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive				ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive				ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive				ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive				ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive				ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive				ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive				ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive				ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive				ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive				ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive				ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive				ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive				ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive				ns
LVCMOS12_4mA	LVCMOS 1.2 4mA drive				ns
PCI33	PCI33				ns

1. Timing adders are characterized but not tested on every device.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		33	420	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		33	420	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.258	210	MHz
f_{VCO}	PLL VCO Frequency		420	840	MHz
f_{PFD}	Phase Detector Input Frequency		33	—	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	default duty cycle selected	45	55	%
t_{OPJIT}	Output Clock Period Jitter	$f_{OUT} \geq 100MHz$	—	+/- 100	ps
		$f_{OUT} < 100MHz$	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	+/- 200	ps
t_W	Output Clock Pulse Width	At 90% or 10%	1	—	ns
t_{LOCK}[1]	PLL Lock-in Time		—	150	us
t_{PA}	Programmable Delay Unit		100	400	ps
t_R/t_F	Input Clock Rise/Fall Time	10% to 90%	—	1	ns
t_{IPJIT}	Input Clock Period Jitter		—	+/- 200	ps
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns

1. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

LatticeECP/EC sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
sysCONFIG Byte Data Flow					
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK		12	—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK		0	—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—			ns
t_{SUCS}	CS[0:1] Setup Time to CCLK		12	—	ns
t_{HCS}	CS[0:1] Hold Time to CCLK		0	—	ns
t_{SUWD}	Write Signal Setup Time to CCLK			—	ns
t_{HWD}	Write Signal Hold Time to CCLK			—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	12		ns
t_{CORD}	Clock to Out for Read Data	—			ns
sysCONFIG Byte Slave Clocking					
t_{BSCH}	Byte Slave Clock Minimum High Pulse		6	—	ns
t_{BSCL}	Byte Slave Clock Minimum Low Pulse		6	—	ns
t_{BSCYC}	Byte Slave Clock Cycle Time		12	—	ns
t_{SUSCDI}	Din Setup time to CCLK Slave Mode		5	—	ns
t_{HSCDI}	Din Hold Time to CCLK Slave Mode		0	—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—	12		ns
sysCONFIG Serial (Bit) Data Flow					
t_{SUMCDI}	Din Setup Time to CCLK Master Mode		5	—	ns
t_{HMCDI}	Din Hold Time to CCLK Master Mode		0	—	ns
sysCONFIG Serial Slave Clocking					
t_{SSCH}	Serial Slave Clock Minimum High Pulse		6	—	ns
t_{SSCL}	Serial Slave Clock Minimum Low Pulse		6	—	ns
sysCONFIG POR, Initialization and Wake Up					
t_{ICFG}	Initialization time of Internal CONFIG Circuit	—	5		ms
t_{VMC}	Time from t_{ICFG} to valid Master Clock	—	5		us
t_{PRGMRJ}	Program Pin Pulse Rejection	—	10		ns
t_{PRGM}	Low time to Start Configuration		25	—	ns
t_{DINIT}	INIT Delay Time		25	—	ns
$t_{DPPINIT}$	Delay Time from Program Low to INIT Low	—			ns
t_{DINITD}	Delay Time from Program Low to Done Low	—	37		ns
t_{IODISS}	User I/O Disable	—			ns
t_{IOENSS}	User I/O Enabled Time from GOE Being Released During Wake-up	—			ns
t_{MWC}	Additional Wake Master Clock Signals After Done Pin High	—	128		Typical cycle
sysCONFIG SPI Port					
t_{CFGX}	Init High to Clock Low	—	80		ns
t_{CSSPI}	Init High to CSSPIN Low	—	2		ns
t_{CSCCLK}	Clock Low to CSSPIN Low	—	0		ns
t_{SOCDO}	Clock Low to Output Valid	—	15		ns
t_{SOSU}	Data Setup Time		5	—	ns
t_{SOE}	CSSPIN Active Setup Time		0	—	ns
t_{CSPID}	CSSPIN Low to First Clock Edge Setup Time		400	—	ns

LatticeECP/EC sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Clock Mode	Min.	Typ.	Max.	Units
Master Clock				
5MHz	3.78	5.4	7.02	MHz
10MHz	7	10	13	MHz
15MHz	10.5	15	19.5	MHz
20MHz	14	20	26	MHz
25MHz	18.2	26	33.8	MHz
30MHz	21	30	39	MHz
35MHz	23.8	34	44.2	MHz
40MHz	28.7	41	53.3	MHz
45MHz	31.5	45	58.5	MHz
50MHz	35.7	51	66.3	MHz
55MHz	38.5	55	71.5	MHz
60MHz	42	60	78	MHz
Duty Cycle	40	—	60	%

JTAG Port Timing Specifications

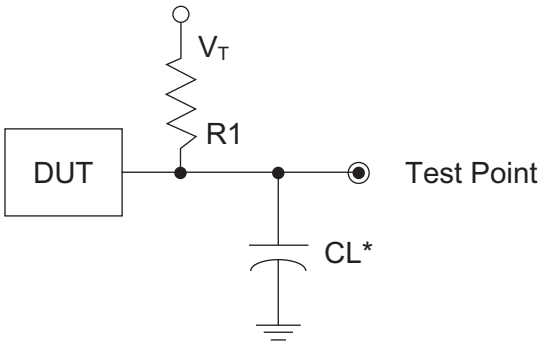
Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK Clock Frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enalbe	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	10	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Switching Test Conditions

Figure 3-12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

Figure 3-12. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	188	0pF	$V_{CCIO}/2$	V_{OL}
LVCMOS 2.5 I/O (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS 2.5 I/O (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS 2.5 I/O (L -> Z)			V_{OL} + 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V_{CC}	—	Power supply pins for core logic. Dedicated pins.
V_{CCAUX}	—	Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated pins.
V_{CCIOx}	—	Power supply pins for I/O bank x. Dedicated pins.
$V_{REF1(x)}$, $V_{REF2(x)}$	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are as assigned V_{REF} inputs. When not used, they may be used as I/O pins.
XRES	—	10K ohm +/-1% resistor must be connected between this pad and ground.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_PLL[T, C]_IN_A	I	Reference clock (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_PLL[T, C]_FB_A	I	Optional feedback (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.
[LOC]DQS[num]	I	DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output.
Test and Programming (Dedicated pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.

Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data out pin used to shift data out of device using 1149.1.
V_{CCJ}	—	V_{CCJ} - The power supply pin for JTAG Test Access Port.
Configuration Pads (used during sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY	I/O	Generally not used.
CSN	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled.
CS1N	I	sysCONFIG chip select (Active Low). During configuration, a pull-up is enabled.
WRITEN	I	Write Data on Parallel port (Active low).
D[7:0]	I/O	sysCONFIG Port Data I/O.
DOUT, CSON	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port.
DI	I	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled.

LFEC20/LFECP20 Pin Information Summary

Pin Type		Package	
		484 fpBGA	672 fpBGA
Single Ended User I/O		360	400
Differential Pair User I/O		180	200
Configuration	Dedicated	12	12
	Muxed	56	56
TAP		5	5
Dedicated (total without supplies)			
V_{CC}		20	32
V_{CCAUX}		12	20
V_{CCIO}	Bank0	4	6
	Bank1	4	6
	Bank2	4	6
	Bank3	4	6
	Bank4	4	6
	Bank5	4	6
	Bank6	4	6
	Bank7	4	6
GND		44	63
NC		3	96
Single Ended/ Differential I/O per Bank	Bank0	48	64
	Bank1	48	48
	Bank2	40	40
	Bank3	44	48
	Bank4	48	48
	Bank5	48	64
	Bank6	44	48
	Bank7	40	40
V_{CCJ}		1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

LFEC20/LFECP20 Power Supply and NC Connections

Signals	484 fpBGA	672 fpBGA
VCC	J6, J7, J16, J17, K6, K7, K16, K17, L6, L17, M6, M17, N6, N7, N16, N17, P6, P7, P16, P17	H8, H9, H10, H11, H16, H17, H18, H19, J9, J18, K8, K19, L8, L19, M19, N7, R7, R20, T19, U8, U19, V8, V18, V9, W8, W9, W10, W11, W16, W17, W18, W19
VCCIO0	G11, H9, H10, H11	H12, H13, J10, J11, J12, J13
VCCIO1	G12, H12, H13, H14	H14, H15, J14, J15, J16, J17
VCCIO2	J15, K15, L15, L16	K17, K18, L18, M18, N18, N19
VCCIO3	M15, M16, N15, P15	P18, P19, R18, R19, T18, U18
VCCIO4	R12, R13, R14, T12	V14, V15, V16, V17, W14, W15
VCCIO5	R9, R10, R11, T11	V10, V11, V12, V13, W12, W13
VCCIO6	M7, M8, N8, P8	P8, P9, R8, R9, T9, U9
VCCIO7	J8, K8, L7, L8	K9, L9, M8, M9, N8, N9
VCCJ	U2	U6
VCCAUX	G7, G8, G15, G16, H7, H16, R7, R16, T7, T8, T15, T16	G13,H7, H20, J8, J19, K7, L20, M7, M20, N20, P7, P20, T7, T8, T20, V7, V19, W20, Y7, Y13
GND	A1, A22, AB1, AB22, H8, H15, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, R8, R15	K10, K11, K12, K13, K14, K15, K16, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17
NC	A2, A21, AB2	A25, B2, B23, B24, B25, B26, C2, C3, C19, C20, C21, C22, C23, C24, D3, D5, D20, D21, D22, D24, E5, E19, E21, E22, E24, E25, E26, F4, F5, F20, F22, F23, F24, F26, G5, G20, G26, H2, H3, H5, H6, H22, J2, J3, J7, J21, J22, J23, W5, W7, Y5, Y6, Y19, Y20, Y21, Y22, Y23, Y24, AA2, AA3, AA4, AA5, AA21, AA22, AA23, AA24, AB3, AB5, AB19, AB20, AB21, AB22, AB23, AB24, AC2, AC3, AC19, AC20, AC21, AC22, AD1, AD2, AD3, AD19, AD20, AD21, AD22, AD23, AD24, AD25, AD26, AE1, AE24, AE25, AE26, AF25

LFEC20/LFECP20 Logic Signal Connections: 484 & 672 fpBGA

Ball Function	Bank	LVDS	Dual Function	484 fpBGA	672 fpBGA
PL2A	7	T	VREF2_7	D4	E3
PL2B	7	C	VREF1_7	E4	E4
PL3A	7	T		C3	B1
PL3B	7	C		B2	C1
PL4A	7	T		E5	F3
PL4B	7	C		F5	G3
PL5A	7	T		D3	D2
PL5B	7	C		C2	E2
PL6A	7	T	LDQS6	F4	D1
PL6B	7	C		G4	E1
PL7A	7	T		E3	F2
PL7B	7	C		D2	G2
PL8A	7	T	LUM0_PLLT_IN_A	B1	F6
PL8B	7	C	LUM0_PLLC_IN_A	C1	G6
PL9A	7	T	LUM0_PLLT_FB_A	F3	H4
PL9B	7	C	LUM0_PLLC_FB_A	E2	G4
PL11A	7	T		G5	J4
PL11B	7	C		H6	J5
PL12A	7	T		G3	K4
PL12B	7	C		H4	K5
PL13A	7	T		J5	J6
PL13B	7	C		H5	K6
PL14A	7	T		F2	F1
PL14B	7	C		F1	G1
PL15A	7	T		E1	H1
PL15B	7	C		D1	J1
PL16A	7	T		H3	K2
PL16B	7	C		G2	K1
PL17A	7	T		H2	K3
PL17B	7	C		G1	L3
PL18A	7	T		J4	L2
PL18B	7	C		J3	L1
PL19A	7	T	LDQS19	J2	M3
PL19B	7	C		H1	M4
PL20A	7	T		K4	M1
PL20B	7	C		K5	M2
PL21A	7	T		K3	L4
PL21B	7	C		K2	L5
PL22A	7	T	PCLKT7_0	J1	N2
PL22B	7	C	PCLKC7_0	K1	N1
XRES	6			L3	N3
PL24A	6	T		L4	P1
PL24B	6	C		L5	P2

LFEC20/LFECP20 Logic Signal Connections: 484 & 672 fpBGA (Cont.)

Ball Function	Bank	LVDS	Dual Function	484 fpBGA	672 fpBGA
PL25A	6	T		L2	L7
PL25B	6	C		L1	L6
PL26A	6	T		M4	N4
PL26B	6	C		M5	N5
PL27A	6	T		M1	R1
PL27B	6	C		M2	R2
PL28A	6	T	LDQS28	N3	P4
PL28B	6	C		M3	P3
PL29A	6	T		N5	M5
PL29B	6	C		N4	M6
PL30A	6	T		N1	T1
PL30B	6	C		N2	T2
PL31A	6	T		P1	R4
PL31B	6	C		P2	R3
PL32A	6	T		R6	N6
PL32B	6	C		P5	P5
PL33A	6	T		P3	P6
PL33B	6	C		P4	R5
PL34A	6	T		R1	U1
PL34B	6	C		R2	U2
PL35A	6	T		R5	T3
PL35B	6	C		R4	T4
PL36A	6	T	LDQS36	T1	R6
PL36B	6	C		T2	T5
PL37A	6	T		R3	T6
PL37B	6	C		T3	U5
PL38A	6	T			U3
PL38B	6	C			U4
PL39A	6	T			V1
PL39B	6	C			V2
TCK	6			T5	U7
TDI	6			U5	V4
TMS	6			T4	V5
TDO	6			U1	V3
VCCJ	6			U2	U6
PL41A	6	T	LLM0_PLLT_IN_A	V1	W1
PL41B	6	C	LLM0_PLLC_IN_A	V2	W2
PL42A	6	T	LLM0_PLLT_FB_A	U3	V6
PL42B	6	C	LLM0_PLLC_FB_A	V3	W6
PL43A	6	T		U4	Y1
PL43B	6	C		V5	Y2
PL44A	6	T		W1	W3
PL44B	6	C		W2	W4
PL45A	6	T	LDQS45	Y1	AA1

LFEC20/LFECP20 Logic Signal Connections: 484 & 672 fpBGA (Cont.)

Ball Function	Bank	LVDS	Dual Function	484 fpBGA	672 fpBGA
PL45B	6	C		Y2	AB1
PL46A	6	T		AA1	Y4
PL46B	6	C		AA2	Y3
PL47A	6	T		W4	AC1
PL47B	6	C		V4	AB2
PL48A	6	T	VREF1_6	W3	AB4
PL48B	6	C	VREF2_6	Y3	AC4
PB2A	5	T			AB6
PB2B	5	C			AA6
PB3A	5	T			AC7
PB3B	5	C			Y8
PB4A	5	T			AB7
PB4B	5	C			AA7
PB5A	5	T			AC6
PB5B	5	C			AC5
PB6A	5	T	BDQS6		AB8
PB6B	5	C			AC8
PB7A	5	T			AE2
PB7B	5	C			AA8
PB8A	5	T			AF2
PB8B	5	C			Y9
PB9A	5	T			AD5
PB9B	5	C			AD4
PB10A	5	T		V7	AD8
PB10B	5	C		T6	AC9
PB11A	5	T		V8	AE3
PB11B	5	C		U7	AB9
PB12A	5	T		W5	AF3
PB12B	5	C		U6	AD9
PB13A	5	T		AA3	AE4
PB13B	5	C		AB3	AF4
PB14A	5	T	BDQS14	Y6	AE5
PB14B	5	C		V6	AA9
PB15A	5	T		AA5	AF5
PB15B	5	C		W6	Y10
PB16A	5	T		Y5	AD6
PB16B	5	C		Y4	AC10
PB17A	5	T		AA4	AF6
PB17B	5	C		AB4	AE6
PB18A	5	T		Y7	AF7
PB18B	5	C		W8	AB10
PB19A	5	T		W7	AE7
PB19B	5	C		U8	AD10
PB20A	5	T		W9	AD7

LFEC20/LFECP20 Logic Signal Connections: 484 & 672 fpBGA (Cont.)

Ball Function	Bank	LVDS	Dual Function	484 fpBGA	672 fpBGA
PB20B	5	C		U9	AA10
PB21A	5	T		Y8	AF8
PB21B	5	C		Y9	AF9
PB22A	5	T	BDQS22	V9	AD11
PB22B	5	C		T9	Y11
PB23A	5	T		W10	AE8
PB23B	5	C		U10	AC11
PB24A	5	T		V10	AF10
PB24B	5	C		T10	AB11
PB25A	5	T		AA6	AE10
PB25B	5	C		AB5	AE9
PB26A	5	T		AA8	AA11
PB26B	5	C		AA7	Y12
PB27A	5	T		AB6	AE11
PB27B	5	C		AB7	AF11
PB28A	5	T		Y10	AF12
PB28B	5	C		W11	AE12
PB29A	5	T		AB8	AD12
PB29B	5	C		AB9	AC12
PB30A	5	T	BDQS30	AA10	AA12
PB30B	5	C		AA9	AB12
PB31A	5	T		Y11	AE13
PB31B	5	C		AA11	AF13
PB32A	5	T	VREF2_5	V11	AD13
PB32B	5	C	VREF1_5	V12	AC13
PB33A	5	T	PCLKT5_0	AB10	AF14
PB33B	5	C	PCLKC5_0	AB11	AE14
PB34A	4	T	WRITEN	Y12	AA13
PB34B	4	C	CS1N	U11	AB13
PB35A	4	T	VREF1_4	W12	AD14
PB35B	4	C	CSN	U12	AA14
PB36A	4	T	VREF2_4	W13	AC14
PB36B	4	C	D7	U13	AB14
PB37A	4	T	D5	AA12	AF15
PB37B	4	C	D6	AB12	AE15
PB38A	4	T	BDQS38	T13	AD15
PB38B	4	C	D4	V13	AC15
PB39A	4	T		W14	AF16
PB39B	4	C	D3	U14	Y14
PB40A	4	T		Y13	AE16
PB40B	4	C	D2	V14	AB15
PB41A	4	T		AA13	AF17
PB41B	4	C	D1	AB13	AE17
PB42A	4	T		AA14	Y15

LFEC20/LFECP20 Logic Signal Connections: 484 & 672 fpBGA (Cont.)

Ball Function	Bank	LVDS	Dual Function	484 fpBGA	672 fpBGA
PB42B	4	C		Y14	AA15
PB43A	4	T		Y15	AD17
PB43B	4	C		W15	Y16
PB44A	4	T		V15	AD18
PB44B	4	C		T14	AC16
PB45A	4	T		AB14	AE18
PB45B	4	C		AB15	AF18
PB46A	4	T	BDQS46	AB16	AD16
PB46B	4	C		AA15	AB16
PB47A	4	T		AB17	AF19
PB47B	4	C		AA16	AA16
PB48A	4	T		AB18	AA17
PB48B	4	C		AA17	Y17
PB49A	4	T		AB19	AF21
PB49B	4	C		AA18	AF20
PB50A	4	T		W16	AE21
PB50B	4	C		U15	AC17
PB51A	4	T		V16	AF22
PB51B	4	C		U16	AB17
PB52A	4	T		Y17	AE22
PB52B	4	C		V17	AA18
PB53A	4	T		AB20	AE19
PB53B	4	C		AA19	AE20
PB54A	4	T	BDQS54	Y16	AA19
PB54B	4	C		W17	Y18
PB55A	4	T		AA20	AF23
PB55B	4	C		Y19	AA20
PB56A	4	T		Y18	AC18
PB56B	4	C		W18	AB18
PB57A	4	T		T17	AF24
PB57B	4	C		U17	AE23
PR48B	3	C	VREF2_3	W20	AC23
PR48A	3	T	VREF1_3	Y20	AC24
PR47B	3	C		AA21	AC25
PR47A	3	T		AB21	AC26
PR46B	3	C		W19	AB25
PR46A	3	T		V19	AA25
PR45B	3	C		Y21	AB26
PR45A	3	T	RDQS45	AA22	AA26
PR44B	3	C	RLM0_PLLC_IN_A	V20	W23
PR44A	3	T	RLM0_PLLT_IN_A	U20	W24
PR43B	3	C	RLM0_PLLC_FB_A	W21	W22
PR43A	3	T	RLM0_PLLT_FB_A	Y22	W21
PR42B	3	C	DI	V21	Y25

LFEC20/LFECP20 Logic Signal Connections: 484 & 672 fpBGA (Cont.)

Ball Function	Bank	LVDS	Dual Function	484 fpBGA	672 fpBGA
PR42A	3	T	DOUT/CSON	W22	Y26
PR41B	3	C	BUSY	U21	W25
PR41A	3	T	D0	V22	W26
CFG2	3			T19	V24
CFG1	3			U19	V21
CFG0	3			U18	V23
PROGRAMN	3			V18	V22
CCLK	3			T20	V20
INITN	3			T21	V25
DONE	3			R20	U20
PR39B	3	C			V26
PR39A	3	T			U26
PR38B	3	C			U24
PR38A	3	T			U25
PR37B	3	C		T18	U23
PR37A	3	T		R17	U22
PR36B	3	C		R19	U21
PR36A	3	T	RDQS36	R18	T21
PR35B	3	C		U22	T25
PR35A	3	T		T22	T26
PR34B	3	C		R21	T22
PR34A	3	T		R22	T23
PR33B	3	C		P20	T24
PR33A	3	T		N20	R23
PR32B	3	C		P19	R25
PR32A	3	T		P18	R24
PR31B	3	C		P21	R26
PR31A	3	T		P22	P26
PR30B	3	C		N21	R21
PR30A	3	T		N22	R22
PR29B	3	C		N19	P25
PR29A	3	T		N18	P24
PR28B	3	C		M21	P23
PR28A	3	T	RDQS28	L20	P22
PR27B	3	C		L21	N26
PR27A	3	T		M20	M26
PR26B	3	C		M18	N21
PR26A	3	T		M19	P21
PR25B	3	C		M22	N23
PR25A	3	T		L22	N22
PR24B	3	C		K22	N25
PR24A	3	T		K21	N24
PR22B	2	C	PCLKC2_0	J22	L26
PR22A	2	T	PCLKT2_0	J21	K26

LFEC20/LFECP20 Logic Signal Connections: 484 & 672 fpBGA (Cont.)

Ball Function	Bank	LVDS	Dual Function	484 fpBGA	672 fpBGA
PR21B	2	C		H22	M22
PR21A	2	T		H21	M23
PR20B	2	C		L19	M25
PR20A	2	T		L18	M24
PR19B	2	C		K20	M21
PR19A	2	T	RDQS19	J20	L21
PR18B	2	C		K19	L22
PR18A	2	T		K18	L23
PR17B	2	C		G22	L25
PR17A	2	T		F22	L24
PR16B	2	C		F21	K25
PR16A	2	T		E22	J25
PR15B	2	C		E21	J26
PR15A	2	T		D22	H26
PR14B	2	C		G21	H25
PR14A	2	T		G20	J24
PR13B	2	C		J18	K21
PR13A	2	T		H19	K22
PR12B	2	C		J19	K20
PR12A	2	T		H20	J20
PR11B	2	C		H17	K23
PR11A	2	T		H18	K24
PR9B	2	C	RUM0_PLLC_FB_A	D21	F25
PR9A	2	T	RUM0_PLLT_FB_A	C22	G25
PR8B	2	C	RUM0_PLLC_IN_A	G19	H23
PR8A	2	T	RUM0_PLLT_IN_A	G18	H24
PR7B	2	C		F20	H21
PR7A	2	T		F19	G21
PR6B	2	C		E20	D26
PR6A	2	T	RDQS6	D20	D25
PR5B	2	C		C21	F21
PR5A	2	T		C20	G22
PR4B	2	C		F18	G24
PR4A	2	T		E18	G23
PR3B	2	C		B22	C26
PR3A	2	T		B21	C25
PR2B	2	C	VREF1_2	E19	E23
PR2A	2	T	VREF2_2	D19	D23
PT57B	1	C		G17	A24
PT57A	1	T		F17	A23
PT56B	1	C		D18	E18
PT56A	1	T		C18	D19
PT55B	1	C		C19	F19

LFEC20/LFECP20 Logic Signal Connections: 484 & 672 fpBGA (Cont.)

Ball Function	Bank	LVDS	Dual Function	484 fpBGA	672 fpBGA
PT55A	1	T		B20	B22
PT54B	1	C		D17	G19
PT54A	1	T	TDQS54	C16	B21
PT53B	1	C		B19	D18
PT53A	1	T		A20	C18
PT52B	1	C		E17	F18
PT52A	1	T		C17	A22
PT51B	1	C		F16	G18
PT51A	1	T		E16	A21
PT50B	1	C		F15	E17
PT50A	1	T		D16	B17
PT49B	1	C		B18	C17
PT49A	1	T		A19	D17
PT48B	1	C		B17	F17
PT48A	1	T		A18	E20
PT47B	1	C		B16	G17
PT47A	1	T		A17	B20
PT46B	1	C		B15	E16
PT46A	1	T	TDQS46	A16	A20
PT45B	1	C		A15	A19
PT45A	1	T		A14	B19
PT44B	1	C		G14	D16
PT44A	1	T		E15	C16
PT43B	1	C		D15	F16
PT43A	1	T		C15	A18
PT42B	1	C		C14	G16
PT42A	1	T		B14	B18
PT41B	1	C		A13	A17
PT41A	1	T		B13	A16
PT40B	1	C		E14	D15
PT40A	1	T		C13	B16
PT39B	1	C		F14	E15
PT39A	1	T		D14	C15
PT38B	1	C		E13	F15
PT38A	1	T	TDQS38	G13	G15
PT37B	1	C		A12	B15
PT37A	1	T		B12	A15
PT36B	1	C		F13	E14
PT36A	1	T		D13	G14
PT35B	1	C	VREF2_1	F12	D14
PT35A	1	T	VREF1_1	D12	E13
PT34B	1	C		F11	F14
PT34A	1	T		C12	C14
PT33B	0	C	PCLKC0_0	A11	B14

LFEC20/LFECP20 Logic Signal Connections: 484 & 672 fpBGA (Cont.)

Ball Function	Bank	LVDS	Dual Function	484 fpBGA	672 fpBGA
PT33A	0	T	PCLKT0_0	A10	A14
PT32B	0	C	VREF1_0	E12	D13
PT32A	0	T	VREF2_0	E11	C13
PT31B	0	C		B11	A13
PT31A	0	T		C11	B13
PT30B	0	C		B9	F13
PT30A	0	T	TDQS30	B10	F12
PT29B	0	C		A9	A12
PT29A	0	T		A8	B12
PT28B	0	C		D11	A11
PT28A	0	T		C10	B11
PT27B	0	C		A7	D12
PT27A	0	T		A6	C12
PT26B	0	C		B7	B10
PT26A	0	T		B8	A10
PT25B	0	C		A5	G12
PT25A	0	T		B6	A9
PT24B	0	C		G10	E12
PT24A	0	T		E10	B9
PT23B	0	C		F10	F11
PT23A	0	T		D10	A8
PT22B	0	C		G9	D11
PT22A	0	T	TDQS22	E9	C11
PT21B	0	C		C9	B8
PT21A	0	T		C8	B7
PT20B	0	C		F9	E11
PT20A	0	T		D9	A7
PT19B	0	C		F8	G11
PT19A	0	T		D7	C7
PT18B	0	C		D8	G10
PT18A	0	T		C7	C6
PT17B	0	C		A4	C10
PT17A	0	T		B4	D10
PT16B	0	C		C4	F10
PT16A	0	T		C5	A6
PT15B	0	C		D6	E10
PT15A	0	T		B5	C9
PT14B	0	C		E6	G9
PT14A	0	T	TDQS14	C6	D9
PT13B	0	C		A3	A5
PT13A	0	T		B3	A4
PT12B	0	C		F6	F9
PT12A	0	T		D5	B6
PT11B	0	C		F7	E9

LFEC20/LFECP20 Logic Signal Connections: 484 & 672 fpBGA (Cont.)

Ball Function	Bank	LVDS	Dual Function	484 fpBGA	672 fpBGA
PT11A	0	T		E8	C8
PT10B	0	C		G6	G8
PT10A	0	T		E7	B5
PT9B	0	C			A3
PT9A	0	T			A2
PT8B	0	C			F8
PT8A	0	T			B4
PT7B	0	C			E8
PT7A	0	T			B3
PT6B	0	C			D8
PT6A	0	T	TDQS6		G7
PT5B	0	C			C4
PT5A	0	T			C5
PT4B	0	C			E7
PT4A	0	T			D4
PT3B	0	C			F7
PT3A	0	T			D6
PT2B	0	C			D7
PT2A	0	T			E6

LatticeECP/EC Family Data Sheet Ordering Information

June 2004 **Advance Data Sheet**

Part Number Description

LFXXX XX – X – X XXXXXX X

Device Family
- Lattice EC (FPGA)
- Lattice ECP (EC FPGA + DSP Blocks)

Logic Capacity
- 1.5K LUTs = 1*
- 3K LUTs = 3*
- 6K LUTs = 6
- 10K LUTs = 10
- 15K LUTs = 15
- 20K LUTs = 20
- 40K LUTs = 40

Supply Voltage
- E = 1.2V

Note: Parts dual marked per table below.

*Not available in the LatticeECP Family.

Grade
- C = Commercial
- I = Industrial

Package
- T100 = 100-pin TQFP*
- T144 = 144-pin TQFP
- Q208 = 208-pin PQFP
- F256 = 256-ball fpBGA
- F484 = 484-ball fpBGA
- F672 = 672-ball fpBGA
- F900 = 900-ball fpBGA

Speed
- 3 = Slowest
- 4
- 5 = Fastest

Ordering Information

LatticeEC Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC1E-3 Q208C	112	-3	PQFP	208	COM	1.5K
LFEC1E-4 Q208C	112	-4	PQFP	208	COM	1.5K
LFEC1E-5 Q208C	112	-5	PQFP	208	COM	1.5K
LFEC1E-3 T144C	97	-3	TQFP	144	COM	1.5K
LFEC1E-4 T144C	97	-4	TQFP	144	COM	1.5K
LFEC1E-5 T144C	97	-5	TQFP	144	COM	1.5K
LFEC1E-3 T100C	65	-3	TQFP	100	COM	1.5K
LFEC1E-4 T100C	65	-4	TQFP	100	COM	1.5K
LFEC1E-5 T100C	65	-5	TQFP	100	COM	1.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC3E-3 F256C	160	-3	fpBGA	256	COM	3.1K
LFEC3E-4 F256C	160	-4	fpBGA	256	COM	3.1K
LFEC3E-5 F256C	160	-5	fpBGA	256	COM	3.1K
LFEC3E-3 Q208C	145	-3	PQFP	208	COM	3.1K
LFEC3E-4 Q208C	145	-4	PQFP	208	COM	3.1K
LFEC3E-5 Q208C	145	-5	PQFP	208	COM	3.1K
LFEC3E-3 T144C	97	-3	TQFP	144	COM	3.1K

LatticeEC Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC3E-4 T144C	97	-4	TQFP	144	COM	3.1K
LFEC3E-5 T144C	97	-5	TQFP	144	COM	3.1K
LFEC3E-3 T100C	65	-3	TQFP	100	COM	3.1K
LFEC3E-4 T100C	65	-4	TQFP	100	COM	3.1K
LFEC3E-5 T100C	65	-5	TQFP	100	COM	3.1K
LFEC6E-3 F484C	224	-3	fpBGA	484	COM	6.1K
LFEC6E-4 F484C	224	-4	fpBGA	484	COM	6.1K
LFEC6E-5 F484C	224	-5	fpBGA	484	COM	6.1K
LFEC6E-3 F256C	192	-3	fpBGA	256	COM	6.1K
LFEC6E-4 F256C	192	-4	fpBGA	256	COM	6.1K
LFEC6E-5 F256C	192	-5	fpBGA	256	COM	6.1K
LFEC6E-3 Q208C	145	-3	PQFP	208	COM	6.1K
LFEC6E-4 Q208C	145	-4	PQFP	208	COM	6.1K
LFEC6E-5 Q208C	145	-5	PQFP	208	COM	6.1K
LFEC6E-3 T144C	97	-3	TQFP	144	COM	6.1K
LFEC6E-4 T144C	97	-4	TQFP	144	COM	6.1K
LFEC6E-5 T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3 F484C	288	-3	fpBGA	484	COM	10.2K
LFEC10E-4 F484C	288	-4	fpBGA	484	COM	10.2K
LFEC10E-5 F484C	288	-5	fpBGA	484	COM	10.2K
LFEC10E-3 F256C	192	-3	fpBGA	256	COM	10.2K
LFEC10E-4 F256C	192	-4	fpBGA	256	COM	10.2K
LFEC10E-5 F256C	192	-5	fpBGA	256	COM	10.2K
LFEC10E-3 Q208C	145	-3	PQFP	208	COM	10.2K
LFEC10E-4 Q208C	145	-4	PQFP	208	COM	10.2K
LFEC10E-5 Q208C	145	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3 F484C	352	-3	fpBGA	484	COM	15.3K
LFEC15E-4 F484C	352	-4	fpBGA	484	COM	15.3K
LFEC15E-5 F484C	352	-5	fpBGA	484	COM	15.3K
LFEC15E-3 F256C	192	-3	fpBGA	256	COM	15.3K
LFEC15E-4 F256C	192	-4	fpBGA	256	COM	15.3K
LFEC15E-5 F256C	192	-5	fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC20E-3 F672C	400	-3	fpBGA	672	COM	19.7K
LFEC20E-4 F672C	400	-4	fpBGA	672	COM	19.7K
LFEC20E-5 F672C	400	-5	fpBGA	672	COM	19.7K
LFEC20E-3 F484C	360	-3	fpBGA	484	COM	19.7K
LFEC20E-4 F484C	360	-4	fpBGA	484	COM	19.7K
LFEC20E-5 F484C	360	-5	fpBGA	484	COM	19.7K

LatticeEC Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC40E-3 F900C	576	-3	fpBGA	900	COM	40.9K
LFEC40E-4 F900C	576	-4	fpBGA	900	COM	40.9K
LFEC40E-5 F900C	576	-5	fpBGA	900	COM	40.9K
LFEC40E-3 F672C	496	-3	fpBGA	672	COM	40.9K
LFEC40E-4 F672C	496	-4	fpBGA	672	COM	40.9K
LFEC40E-5 F672C	496	-5	fpBGA	672	COM	40.9K

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP6E-3 F484C	224	-3	fpBGA	484	COM	6.1K
LFECP6E-4 F484C	224	-4	fpBGA	484	COM	6.1K
LFECP6E-5 F484C	224	-5	fpBGA	484	COM	6.1K
LFECP6E-3 F256C	192	-3	fpBGA	256	COM	6.1K
LFECP6E-4 F256C	192	-4	fpBGA	256	COM	6.1K
LFECP6E-5 F256C	192	-5	fpBGA	256	COM	6.1K
LFECP6E-3 Q208C	145	-3	PQFP	208	COM	6.1K
LFECP6E-4 Q208C	145	-4	PQFP	208	COM	6.1K
LFECP6E-5 Q208C	145	-5	PQFP	208	COM	6.1K
LFECP6E-3 T144C	97	-3	TQFP	144	COM	6.1K
LFECP6E-4 T144C	97	-4	TQFP	144	COM	6.1K
LFECP6E-5 T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP10E-3 F484C	288	-3	fpBGA	484	COM	10.2K
LFECP10E-4 F484C	288	-4	fpBGA	484	COM	10.2K
LFECP10E-5 F484C	288	-5	fpBGA	484	COM	10.2K
LFECP10E-3 F256C	192	-3	fpBGA	256	COM	10.2K
LFECP10E-4 F256C	192	-4	fpBGA	256	COM	10.2K
LFECP10E-5 F256C	192	-5	fpBGA	256	COM	10.2K
LFECP10E-3 Q208C	145	-3	PQFP	208	COM	10.2K
LFECP10E-4 Q208C	145	-4	PQFP	208	COM	10.2K
LFECP10E-5 Q208C	145	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP15E-3 F484C	352	-3	fpBGA	484	COM	15.3K
LFECP15E-4 F484C	352	-4	fpBGA	484	COM	15.3K
LFECP15E-5 F484C	352	-5	fpBGA	484	COM	15.3K
LFECP15E-3 F256C	192	-3	fpBGA	256	COM	15.3K
LFECP15E-4 F256C	192	-4	fpBGA	256	COM	15.3K
LFECP15E-5 F256C	192	-5	fpBGA	256	COM	15.3K

LatticeECP Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP20E-3 F676C	400	-3	fpBGA	676	COM	19.7K
LFECP20E-4 F676C	400	-4	fpBGA	676	COM	19.7K
LFECP20E-5 F676C	400	-5	fpBGA	676	COM	19.7K
LFECP20E-3 F484C	360	-3	fpBGA	484	COM	19.7K
LFECP20E-4 F484C	360	-4	fpBGA	484	COM	19.7K
LFECP20E-5 F484C	360	-5	fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP40E-3 F896C	576	-3	fpBGA	896	COM	40.9K
LFECP40E-4 F896C	576	-4	fpBGA	896	COM	40.9K
LFECP40E-5 F896C	576	-5	fpBGA	896	COM	40.9K
LFECP40E-3 F676C	496	-3	fpBGA	676	COM	40.9K
LFECP40E-4 F676C	496	-4	fpBGA	676	COM	40.9K
LFECP40E-5 F676C	496	-5	fpBGA	676	COM	40.9K

LatticeEC Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC1E-3 Q208I	112	-3	PQFP	208	IND	1.5K
LFEC1E-4 Q208I	112	-4	PQFP	208	IND	1.5K
LFEC1E-3 T144I	97	-3	TQFP	144	IND	1.5K
LFEC1E-4 T144I	97	-4	TQFP	144	IND	1.5K
LFEC1E-3 T100I	65	-3	TQFP	100	IND	1.5K
LFEC1E-4 T100I	65	-4	TQFP	100	IND	1.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC3E-3 F256I	160	-3	fpBGA	256	IND	3.1K
LFEC3E-4 F256I	160	-4	fpBGA	256	IND	3.1K
LFEC3E-3 Q208I	145	-3	PQFP	208	IND	3.1K
LFEC3E-4 Q208I	145	-4	PQFP	208	IND	3.1K
LFEC3E-3 T144I	97	-3	TQFP	144	IND	3.1K
LFEC3E-4 T144I	97	-4	TQFP	144	IND	3.1K
LFEC3E-3 T100I	65	-3	TQFP	100	IND	3.1K
LFEC3E-4 T100I	65	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-3 F484I	224	-3	fpBGA	484	IND	6.1K
LFEC6E-4 F484I	224	-4	fpBGA	484	IND	6.1K
LFEC6E-3 F256I	192	-3	fpBGA	256	IND	6.1K
LFEC6E-4 F256I	192	-4	fpBGA	256	IND	6.1K
LFEC6E-3 Q208I	145	-3	PQFP	208	IND	6.1K
LFEC6E-4 Q208I	145	-4	PQFP	208	IND	6.1K
LFEC6E-3 T144I	97	-3	TQFP	144	IND	6.1K

LatticeEC Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC1E-3 Q208I	112	-3	PQFP	208	IND	1.5K
LFEC1E-4 Q208I	112	-4	PQFP	208	IND	1.5K
LFEC1E-3 T144I	97	-3	TQFP	144	IND	1.5K
LFEC1E-4 T144I	97	-4	TQFP	144	IND	1.5K
LFEC1E-3 T100I	65	-3	TQFP	100	IND	1.5K
LFEC1E-4 T100I	65	-4	TQFP	100	IND	1.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-4 T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3 F484I	288	-3	fpBGA	484	IND	10.2K
LFEC10E-4 F484I	288	-4	fpBGA	484	IND	10.2K
LFEC10E-3 F256I	192	-3	fpBGA	256	IND	10.2K
LFEC10E-4 F256I	192	-4	fpBGA	256	IND	10.2K
LFEC10E-3 P208I	145	-3	PQFP	208	IND	10.2K
LFEC10E-4 P208I	145	-4	PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3 F484I	352	-3	fpBGA	484	IND	15.3K
LFEC15E-4 F484I	352	-4	fpBGA	484	IND	15.3K
LFEC15E-3 F256I	192	-3	fpBGA	256	IND	15.3K
LFEC15E-4 F256I	192	-4	fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC20E-3 F672I	400	-3	fpBGA	672	IND	19.7K
LFEC20E-4 F672I	400	-4	fpBGA	672	IND	19.7K
LFEC20E-3 F484I	360	-3	fpBGA	484	IND	19.7K
LFEC20E-4 F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC40E-3 F900I	576	-3	fpBGA	900	IND	40.9K
LFEC40E-4 F900I	576	-4	fpBGA	900	IND	40.9K
LFEC40E-3 F672I	496	-3	fpBGA	672	IND	40.9K
LFEC40E-4 F672I	496	-4	fpBGA	672	IND	40.9K

LatticeECP Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP6E-3 F484I	224	-3	fpBGA	484	IND	6.1K
LFECP6E-4 F484I	224	-4	fpBGA	484	IND	6.1K
LFECP6E-3 F256I	192	-3	fpBGA	256	IND	6.1K
LFECP6E-4 F256I	192	-4	fpBGA	256	IND	6.1K
LFECP6E-3 Q208I	145	-3	PQFP	208	IND	6.1K

LatticeECP Industrial (Continued)

LFECP6E-4 Q208I	145	-4	PQFP	208	IND	6.1K
LFECP6E-3 T144I	97	-3	TQFP	144	IND	6.1K
LFECP6E-4 T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP10E-3 F484I	288	-3	fpBGA	484	IND	10.2K
LFECP10E-4 F484I	288	-4	fpBGA	484	IND	10.2K
LFECP10E-3 F256I	192	-3	fpBGA	256	IND	10.2K
LFECP10E-4 F256I	192	-4	fpBGA	256	IND	10.2K
LFECP10E-3 Q208I	145	-3	PQFP	208	IND	10.2K
LFECP10E-4 Q208I	145	-4	PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP15E-3 F484I	352	-3	fpBGA	484	IND	15.3K
LFECP15E-4 F484I	352	-4	fpBGA	484	IND	15.3K
LFECP15E-3 F256I	192	-3	fpBGA	256	IND	15.3K
LFECP15E-4 F256I	192	-4	fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP20E-3 F676I	400	-3	fpBGA	676	IND	19.7K
LFECP20E-4 F676I	400	-4	fpBGA	676	IND	19.7K
LFECP20E-3 F484I	360	-3	fpBGA	484	IND	19.7K
LFECP20E-4 F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP40E-3 F896I	576	-3	fpBGA	896	IND	40.9K
LFECP40E-4 F896I	576	-4	fpBGA	896	IND	40.9K
LFECP40E-3 F676I	496	-3	fpBGA	676	IND	40.9K
LFECP40E-4 F676I	496	-4	fpBGA	676	IND	40.9K

LatticeECP/EC Family Data Sheet Supplemental Information

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For Further Information

A variety of technical notes for the LatticeECP/EC family are available on the Lattice web site at www.latticesemi.com.

- LatticeECP/EC sysIO Usage Guide (TN1056)
- ispTRACY Internal Logic Analyzer Guide (TN1054)
- LatticeECP/EC sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC Devices (TN1051)
- LatticeECP/EC DDR Usage Guide (TN1050)
- Estimating Power Using Power Calculator for LatticeECP/EC Devices (TN1052)
- sysDSP/MAC Usage Guide (TN1057)
- LatticeECP/EC sysCONFIG Usage Guide (TN1053)
- IEEE 1149.1 Boundary Scan Testability in Lattice Devices

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: ww.pcisig.com